Biwa Block Diagram

Project code: 91.4H001.001
PCB P/N : 55.4H001.XXX
REVISION : 06237-2(GCE, Hannstar)

-2-0226

CLK GEN.
ICS 9LPR502
(RTM875T-605) 3

Mobile CPU
Merom 479
2G/2.33G
2.0G : B0, QLYV
2.2G : B0, QLFS
4, 5

G792 20

HOST BUS 800MHz@1.05V

DDR2 533/667 MHz 12,13
533/667MHz

DDR2 533/667 MHz 12,13
533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.M02, B0, QN12
6,7,8,9,10,11

SVIDEO/COMP → TVOUT 15
LVDS → 14" WXGA LCD 14
RGB CRT → CRT 15

X4 DMI
400M Byte/s
C-Link0

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U, B1, QN23
16,17,18,19

Line In 30
Mic In 30
INT.MIC
INT.SPKR 30
Line Out (No-SPDIF) 30

Codec ALC268 29
AZALIA

OP AMP APA2031 30
G1412 30
MODEM MDC Card 22
RJ11 24

PCI BUS

TI 7412 CardBus 1394 CardReader 25,26
PCMCIA I/F
PWR SW TPS2211 27
PCMCIA SLOT Support TypeII 27
1394 CONN 26
MS/MS Pro/xD/ MMC/SD/SDIO 6 in 1 27

LAN Giga LAN BCM5787MKMLG 23
TXFM 24
RJ45 24

New card 28
PWR SW P2231NFC 28

PCIex1
Mini Card Kedron a/b/g/n 28

C Link1

LPC BUS

SATA
PATA

HDD 21
USB 4 PORT 22
CCD 14
CDROM 21
MINI USB 22 Blue-tooth
Finger PT 22

Super I/O Winbond PC87381 33
FIR 32

KBC Winbond WPC8763L 31
SPI I/F
BIOS 33 W25X80-VSSI-G
Touch Pad 32
INT. KB 32

LPC DEBUG CONN. 33

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

CPU DC/DC MAX8770 36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

SYSTEM DC/DC ISL6236 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A) 5V_AUX_S5

SYSTEM DC/DC MAX8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(13A) 1D8V_S3(10A)

G971 39	
1D8V_S3	1D5V_S0 (4A)

APL5913 39	
1D8V_S3	1D25V_S0 (1.5A)

G2997F6U 39	
1D8V_S3	DDR_VREF_S0 (1.2A) DDR_VREF_S3

G909 34	
5V_AUX_S5	3D3V_AUX_S5 (100mA)

MAXIM CHARGER ISL6255 40	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 19V 4.0A UP+5V 5V 100mA

55.4H001.S03G

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Title: ***BLOCK DIAGRAM***
Size: A3 | Document Number: Biwa | Rev: -2
Date: Thursday, March 01, 2007 | Sheet 1 of 42

ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	USB4
4	MINIC1
5	BT
6	CCD
7	Finger
8	NEW
9	NC

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K (?)
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K (?)
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

2007/02/16
1.Page 33: Add SIO 87381 for FIR Issue.
2.Page 31, change KBC from 8768L to 8763L.
3.Page 33, del U33(LPC golden Finger).
4.Page 24/32, change ERC1/ERC2 due to 77.61021.02L is Obsoleted Part !
5.Page 37, del TC22/TC19.
6.Page 38, del TC1/TC4.
==========
2007/02/09
1.Page 14:Modify "Q14" "BTBTN1" "WLBTN1" symbol.
2.Page 36, 37, 38: Replace 0ohm with 0ohm pad.
==========
2007/02/08a
1.Page 14:Modify R428 to"FRONT_PWRLED#_1"and RN58 pin7 to"STBY_LED#_2"due to LED brightness issue.
2.Page 38:Replace "TC26" with "77.C1561.01L".
==========
2007/02/08
1.Page 10:Replace "R244" with "0603-PAD".
2.Page 36:Replace open power gap with close power gap.
3.Page 38:Add capacitor "TC26" for acoustic noise
==========

55.4H001.S03G

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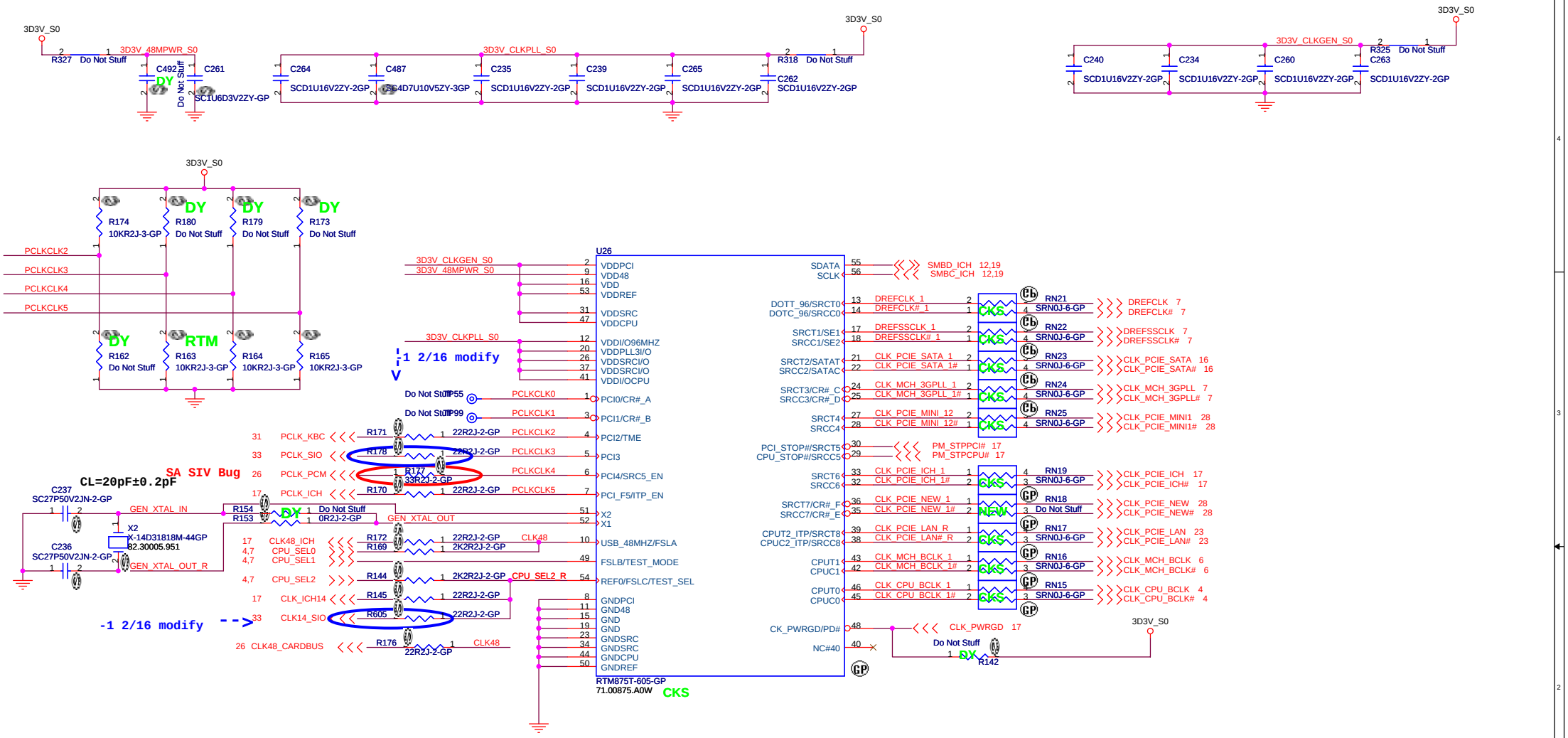
Title: Reference
Size: A3 | Document Number: Biwa | Rev: -2
Date: Thursday, March 01, 2007 | Sheet 2 of 42



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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Title: **Clock Generator**

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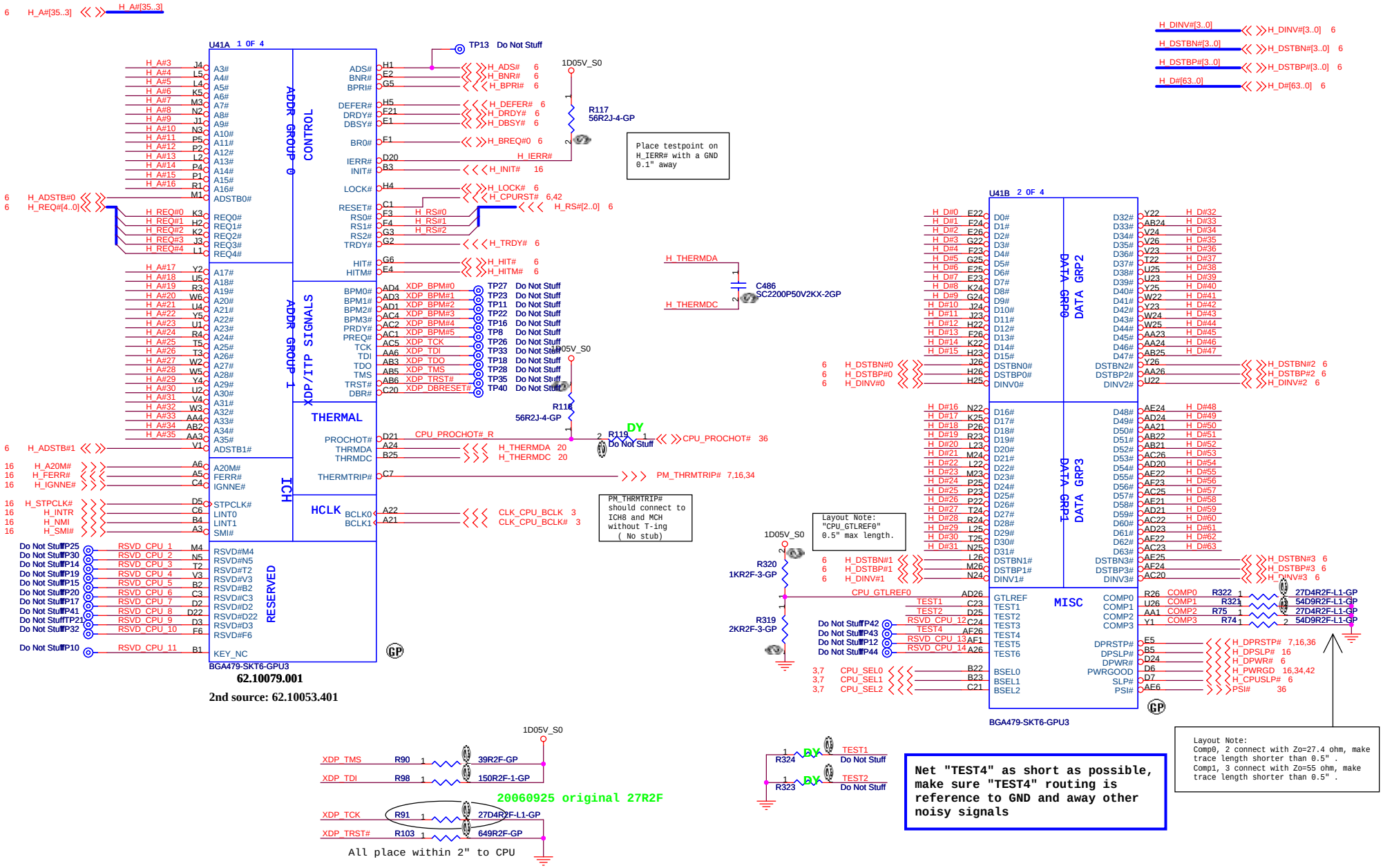

62.10079.001

2nd source: 62.10053.401

55.4H001.S03G

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Title: CPU (1 of 2)

Size | Document Number: Biwa | Rev: SA

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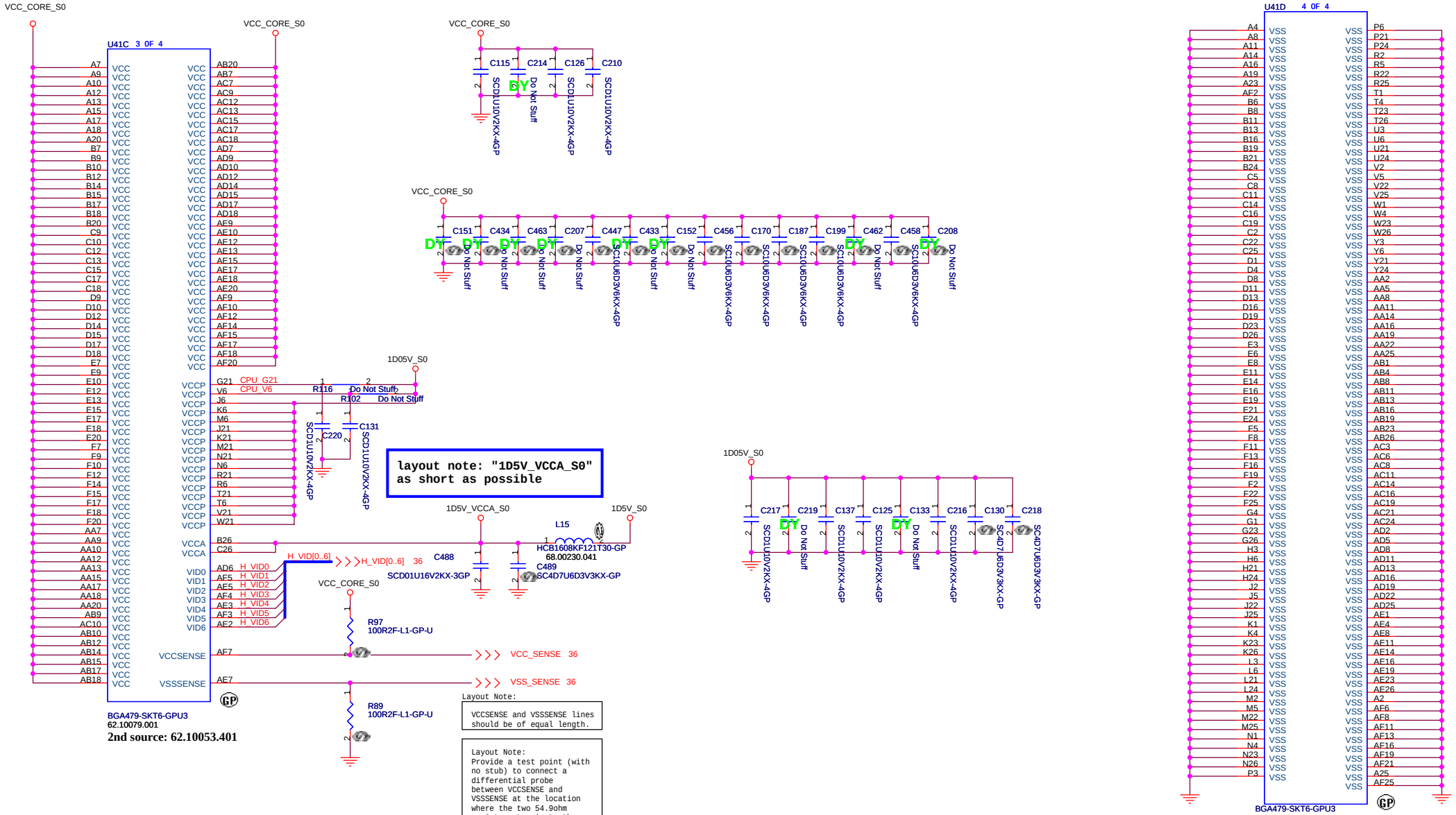

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Title: ***CPU (2 of 2)***

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	Biwa	SA

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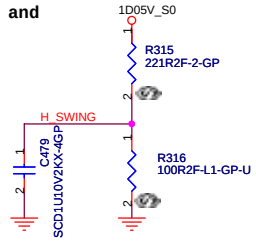
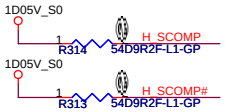
H_SWING routing Trace width and Spacing use 10 / 20 mil

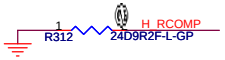
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

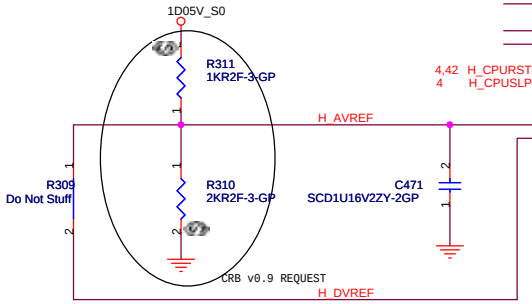


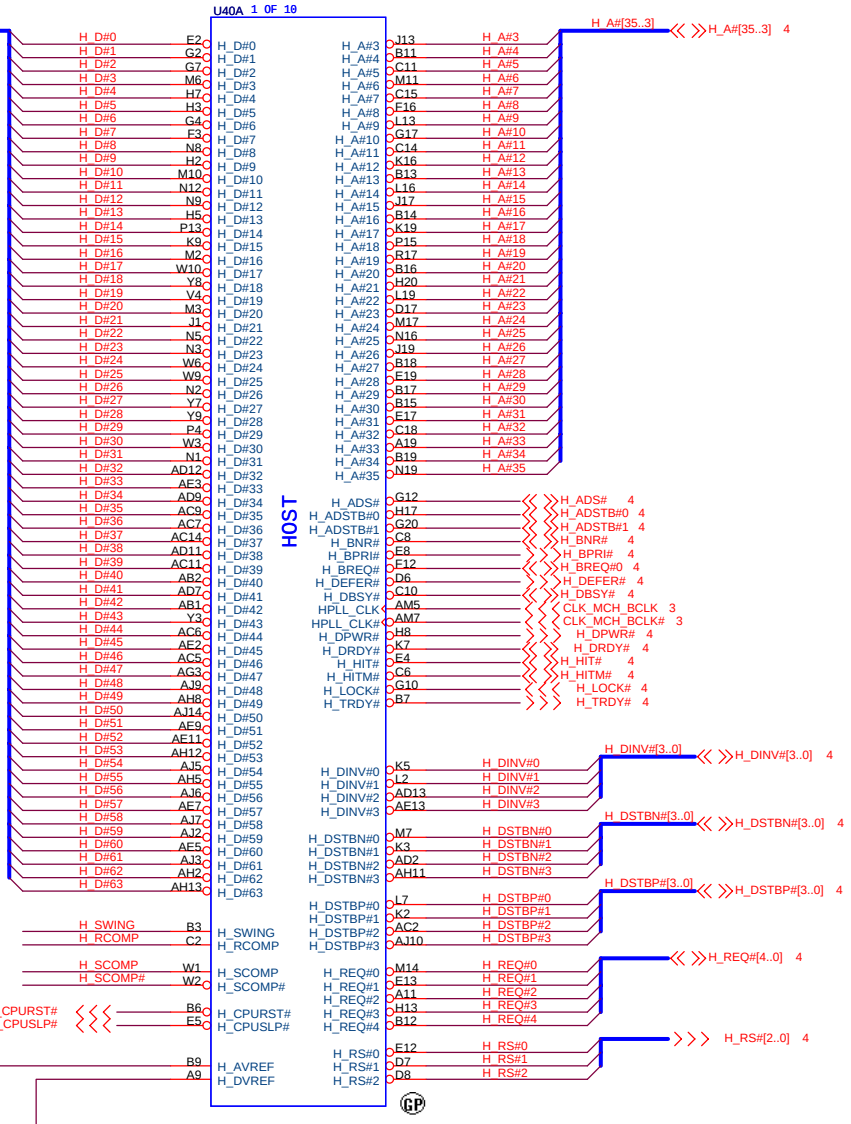
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





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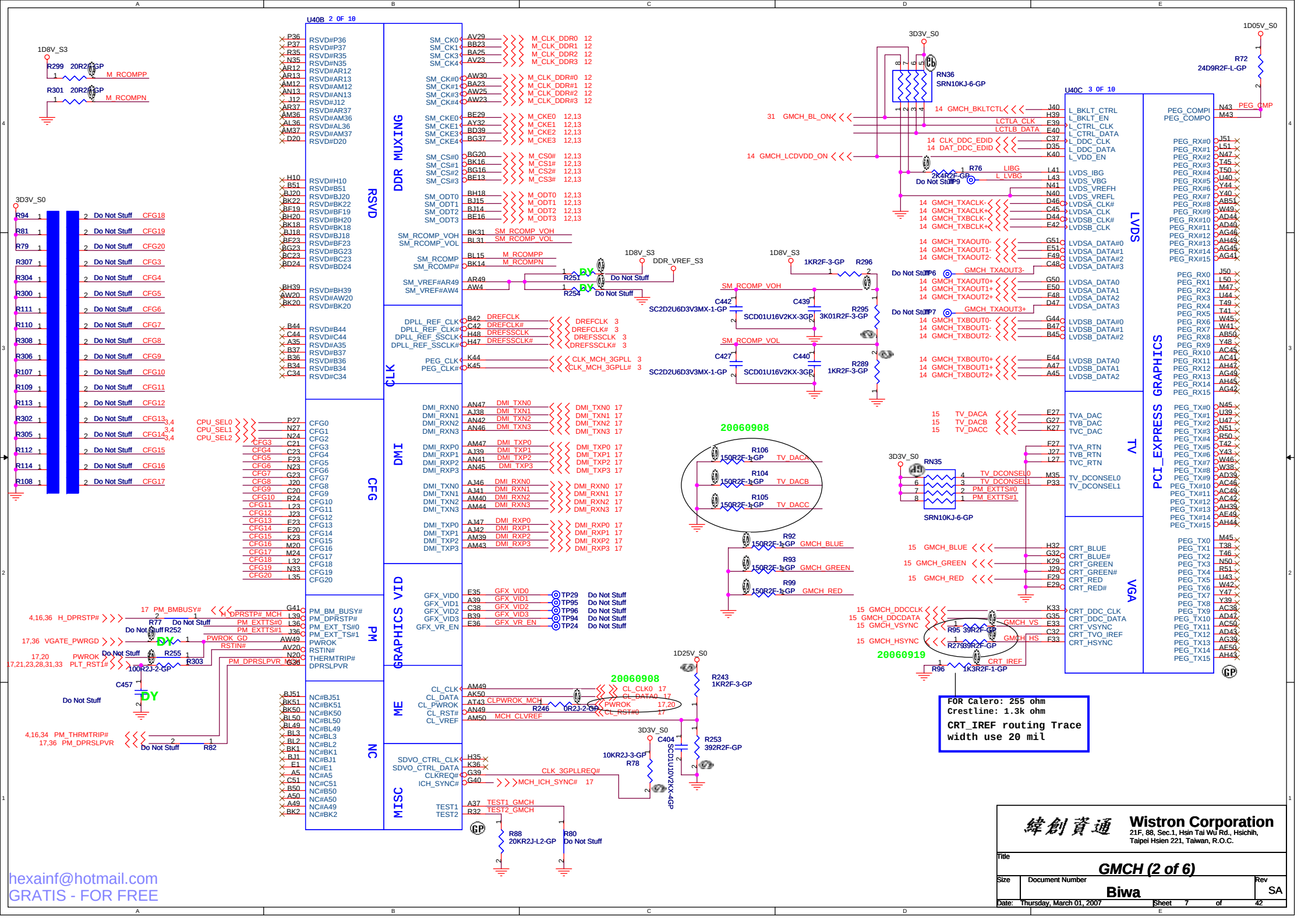
Title: ***GMCH (1 of 6)***

Size | Document Number: **Biwa** | Rev: SA

Date: Thursday, March 01, 2007 | Sheet 6 of 42


U40B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
U40C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
1D8V_S3
3D3V_S0
1D05V_S0
1D25V_S0
1D8V_S3
DDR_VREF_S3
20060908
20060919
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
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Title
GMCH (2 of 6)
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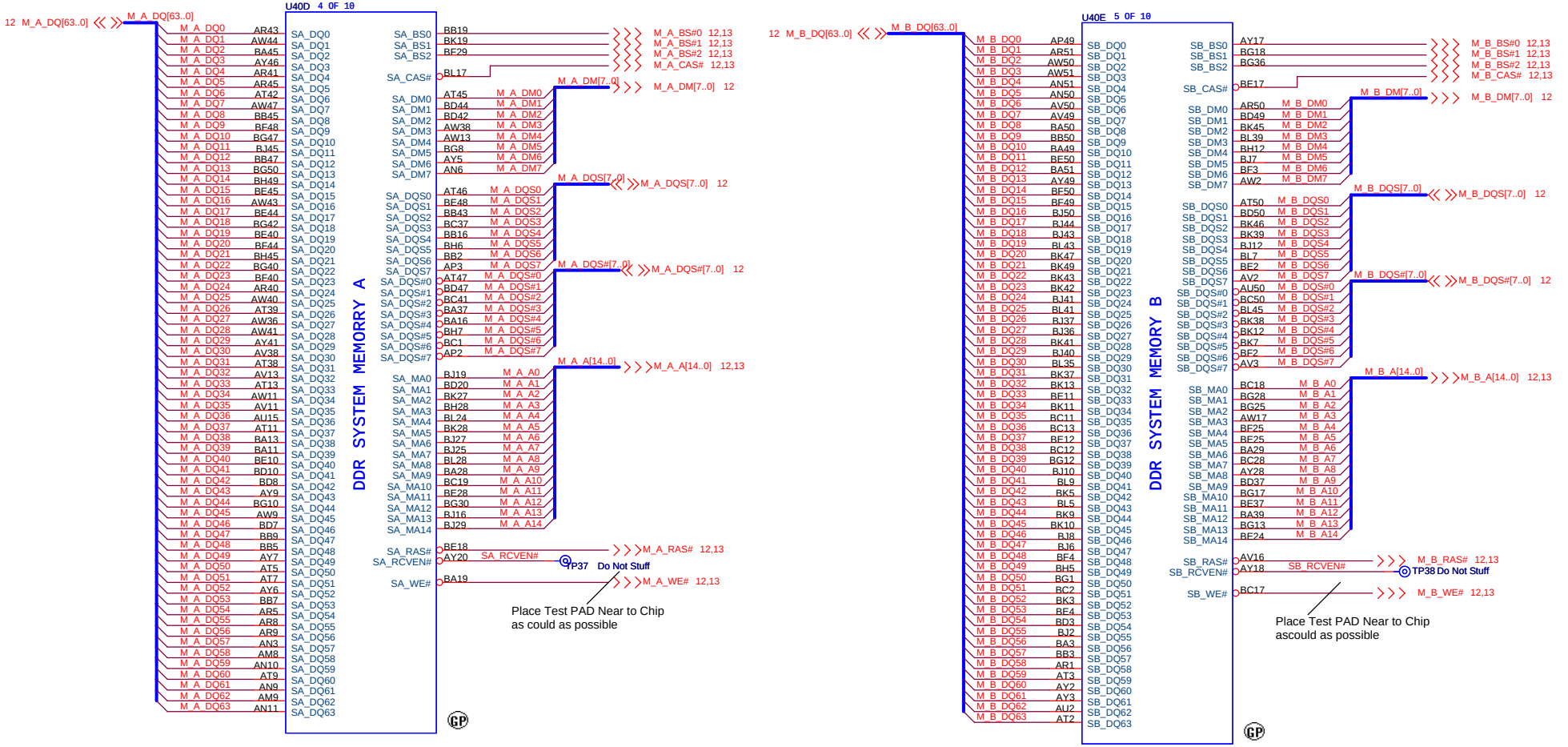

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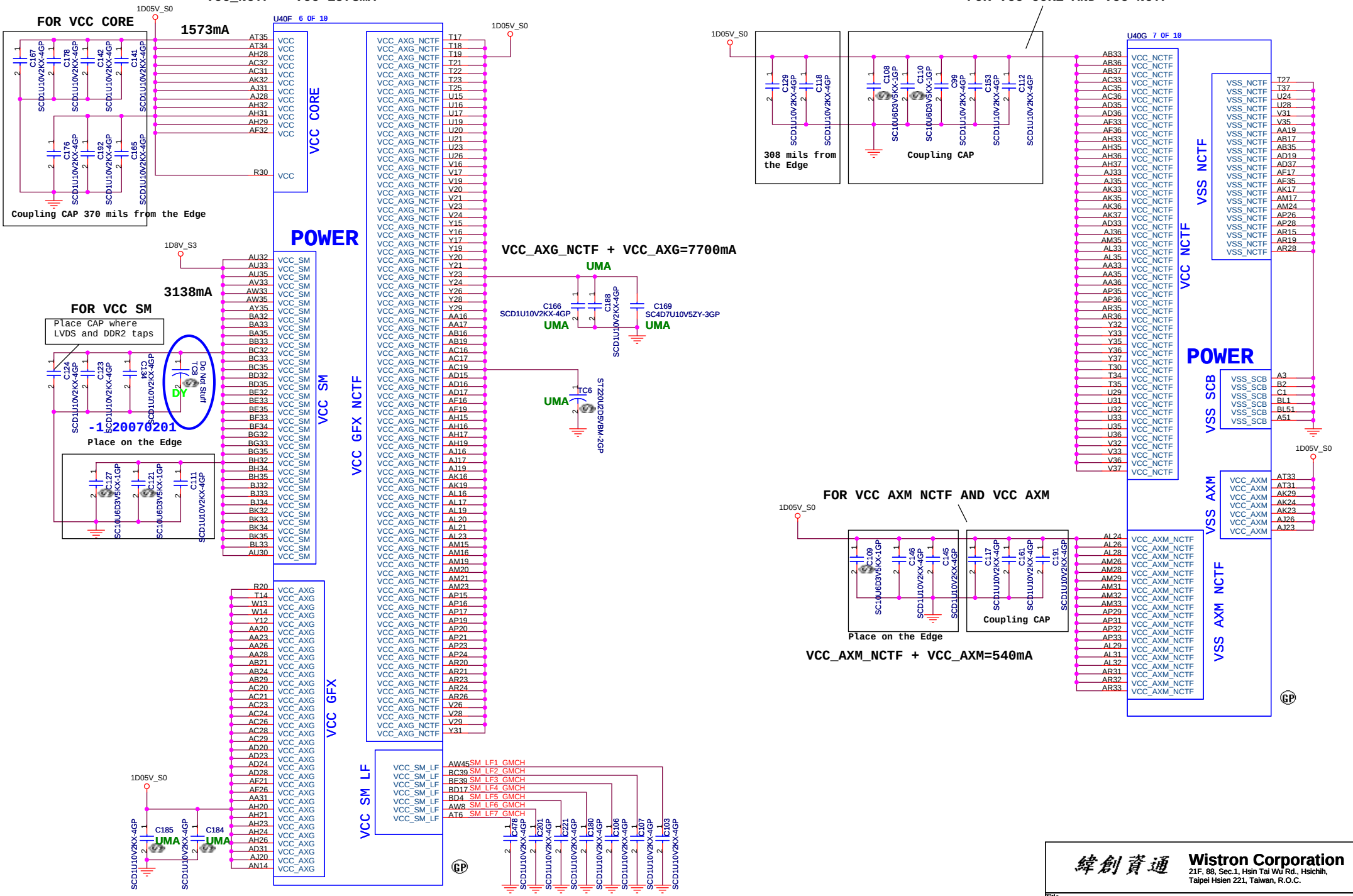

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Title	*GMCH (4 of 6)*	
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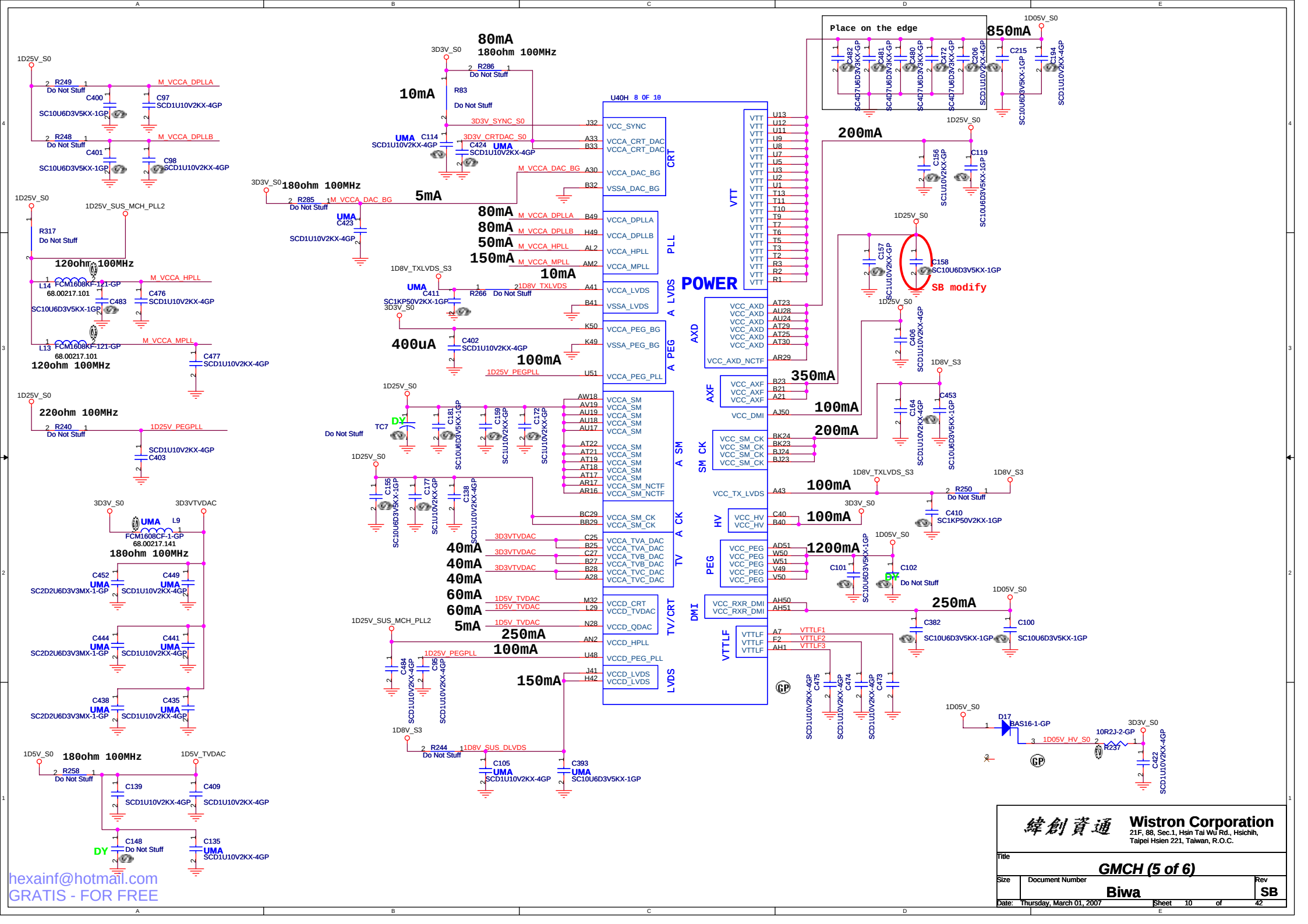
Place on the edge
850mA
200mA
SB modify
80mA
180ohm 100MHz
10mA
5mA
400uA
100mA
150mA
50mA
60mA
40mA
250mA
350mA
1200mA
U40H 8 OF 10
POWER
CRT
PLL
LVDS
SM CK
TV
TV/CRT
DMI
AXD
AXF
PEG
HV
VTT
VTTLF
Do Not Stuff
UMA
DY
GP
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GMCH (5 of 6)
Biwa
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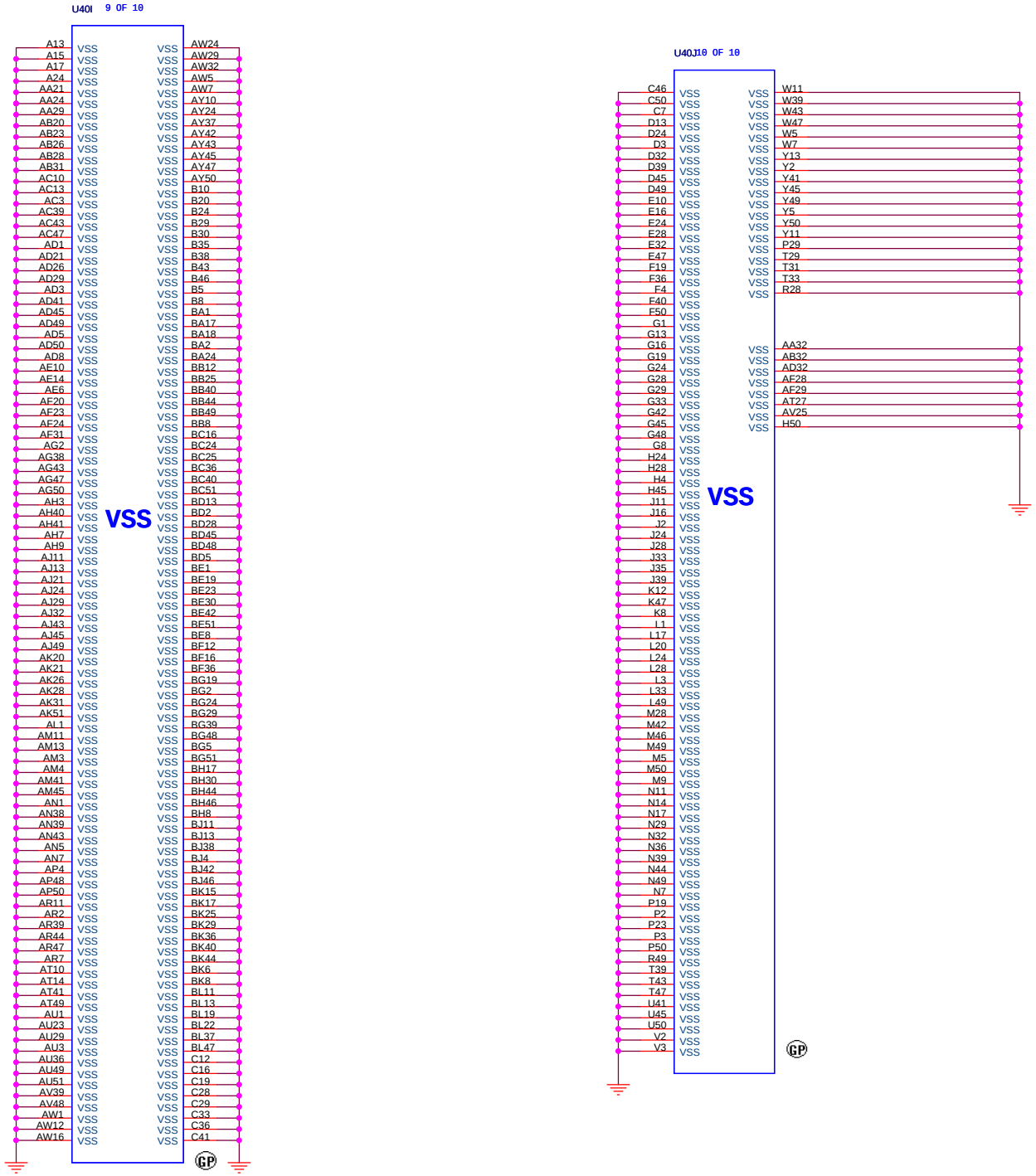

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Title: ***GMCH (6 of 6)***

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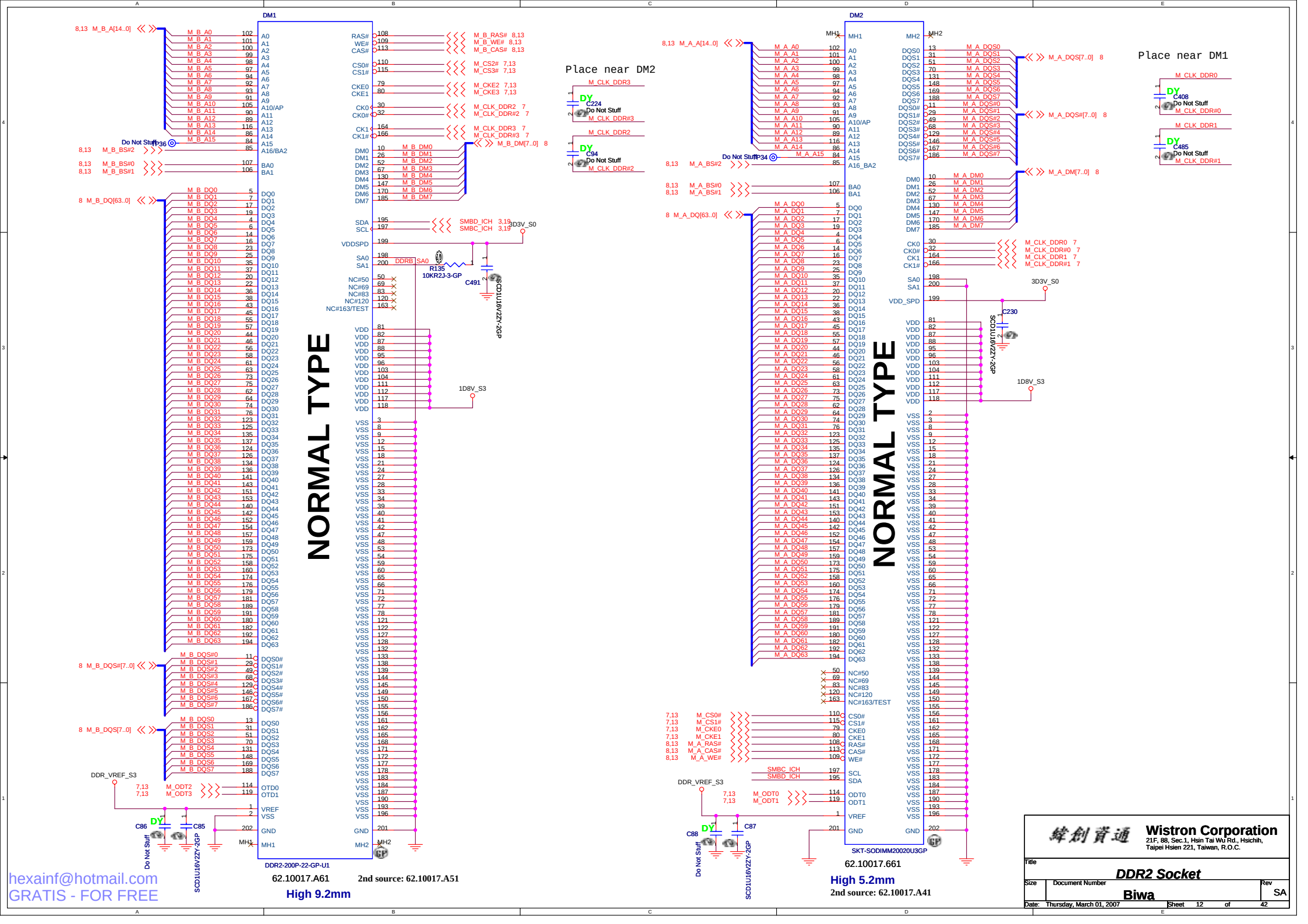
DM1
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
2nd source: 62.10017.A51
High 9.2mm
DM2
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
High 5.2mm
2nd source: 62.10017.A41
Place near DM2
Place near DM1
Do Not Stuff
R135
10KR2J-3-GP
C491
C224
C94
C408
C485
C230
C86
C85
C88
C87
SCD1U16V2ZY-2GP
DDR_VREF_S3
3D3V_S0
1D8V_S3
hexainf@hotmail.com
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Title
DDR2 Socket
Size
Document Number
Biwa
Rev
SA
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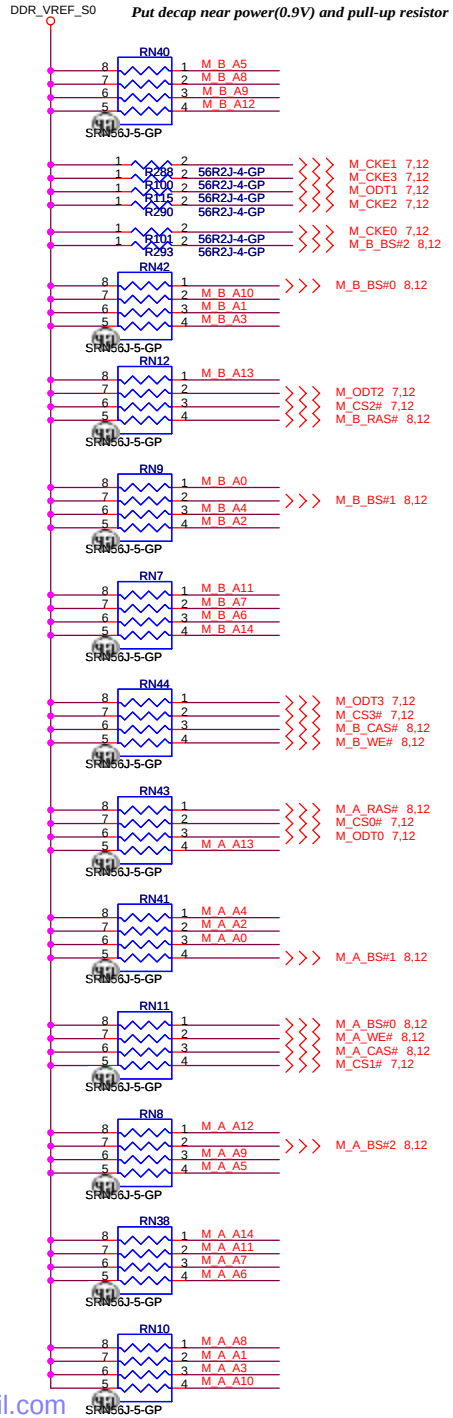
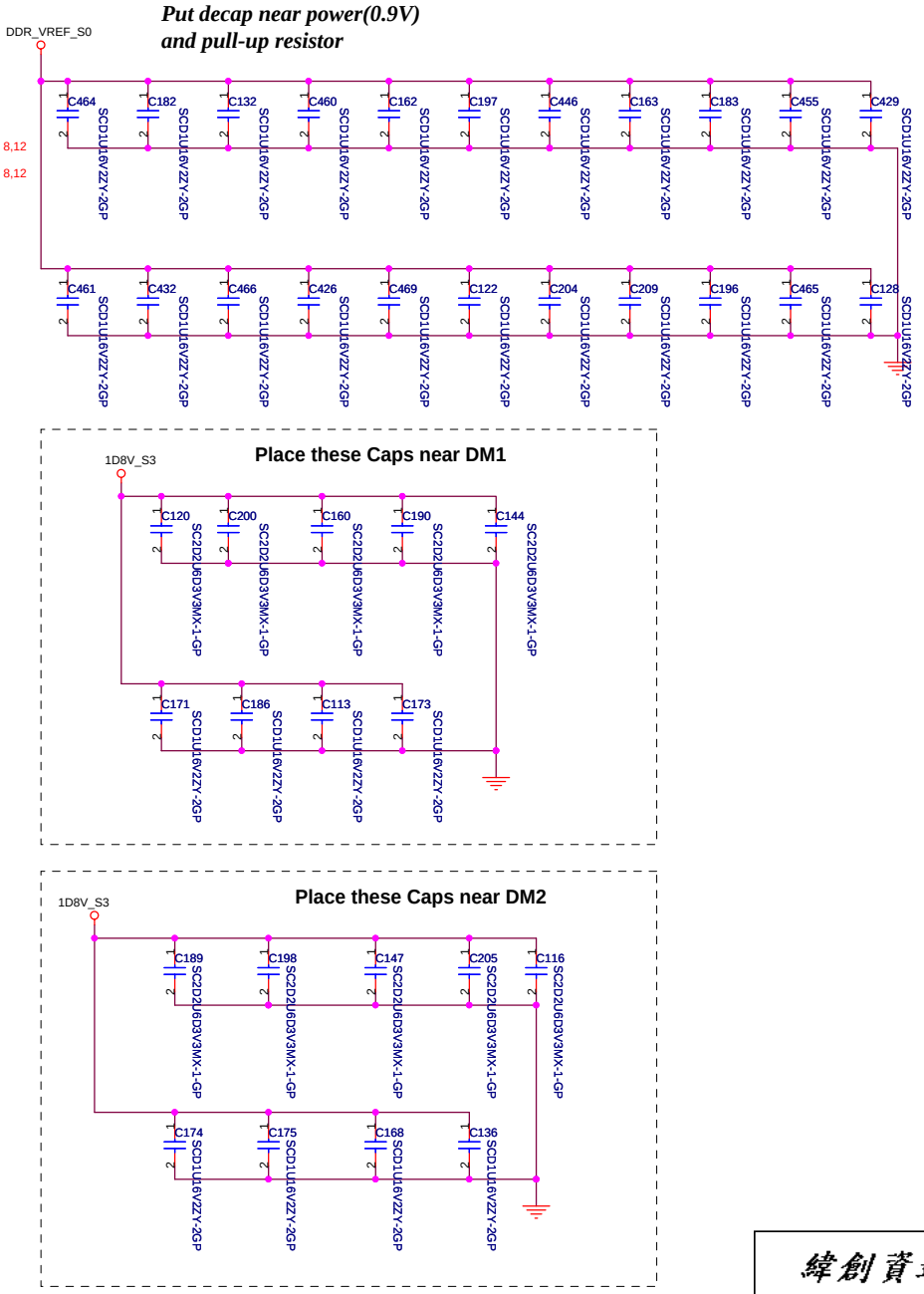
PARALLEL TERMINATION



M_A_A[14..0] ≪ ≫ M_A_A[14..0] 8,12

M_B_A[14..0] ≪ ≫ M_B_A[14..0] 8,12

Decoupling Capacitor



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Title: ***DDR2 Termination Resistor***

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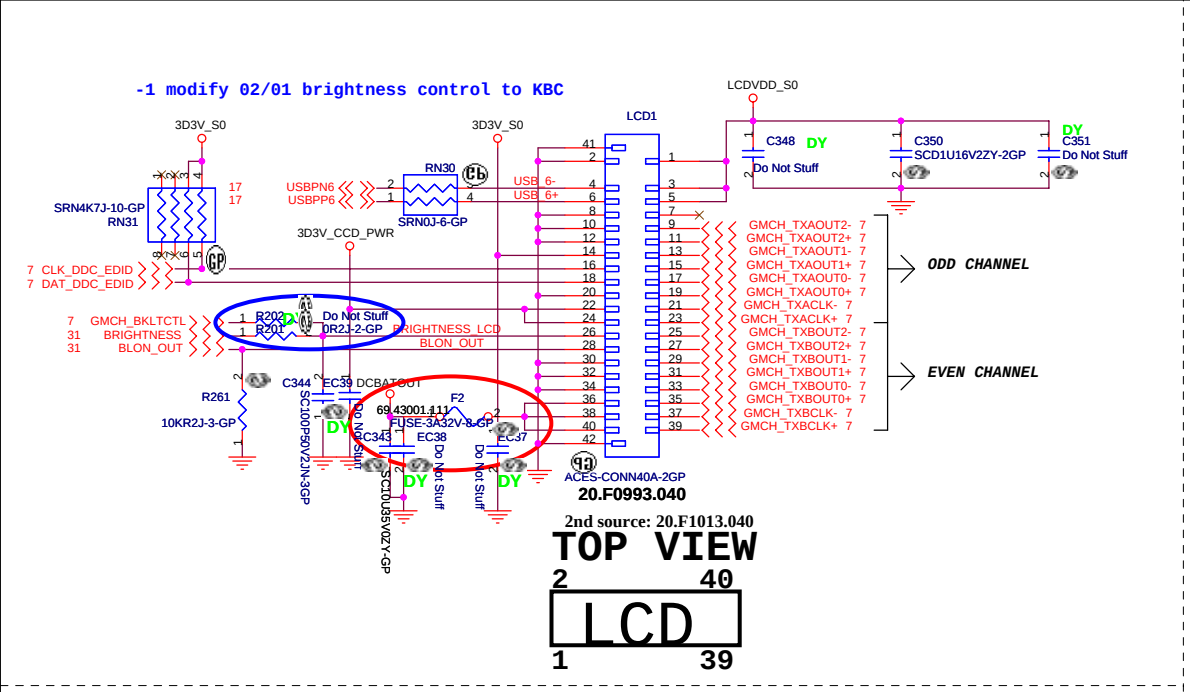

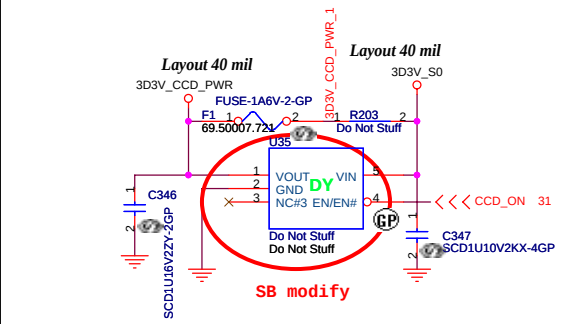

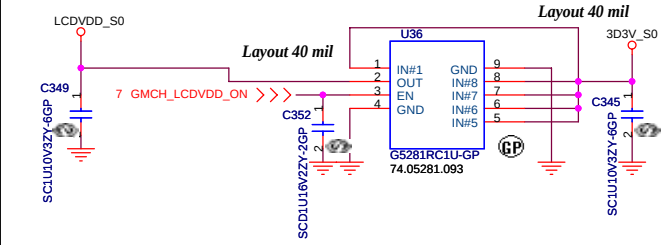

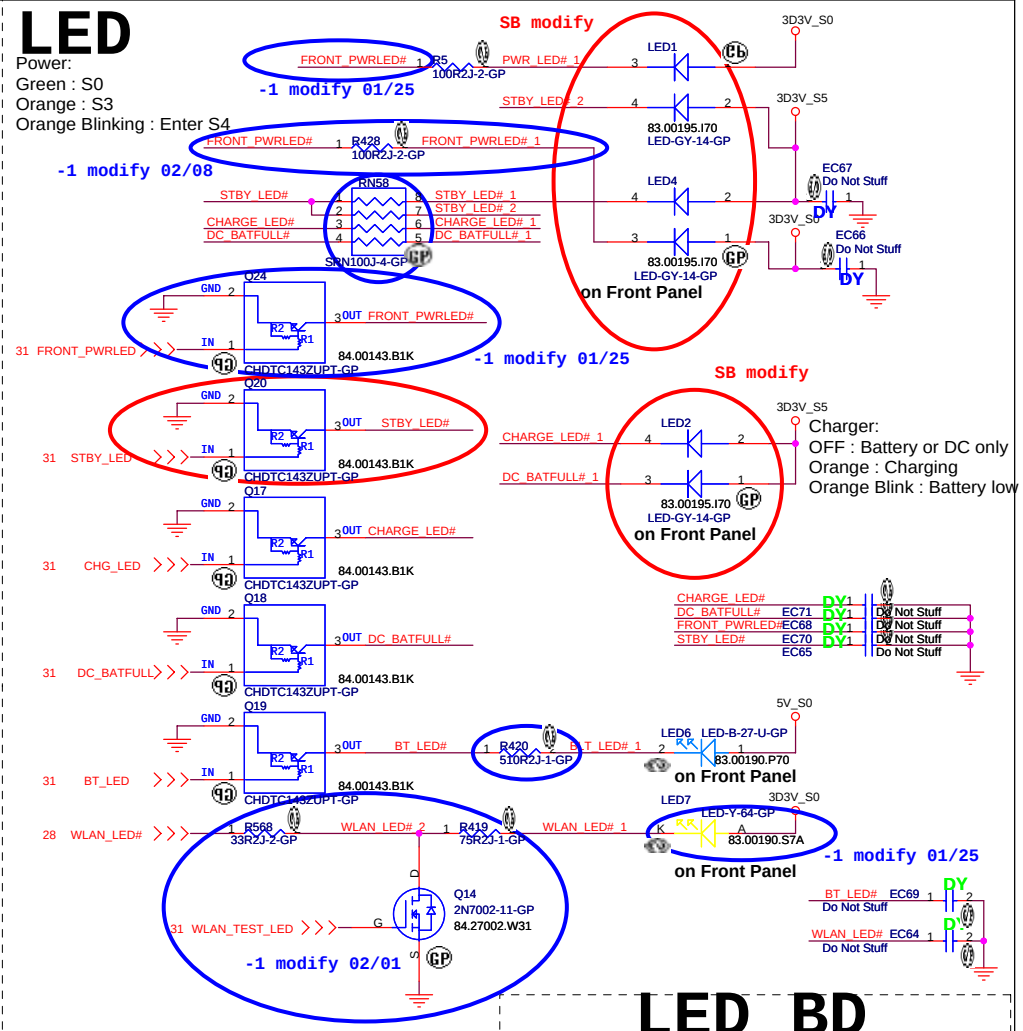

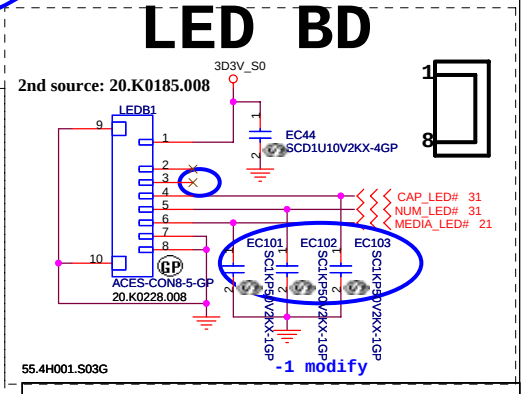

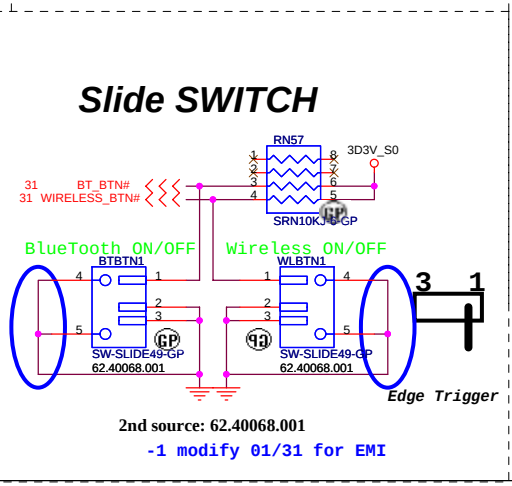

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Title: LCD CONN & LED

Size	Document Number	Rev
	Biwa	-1

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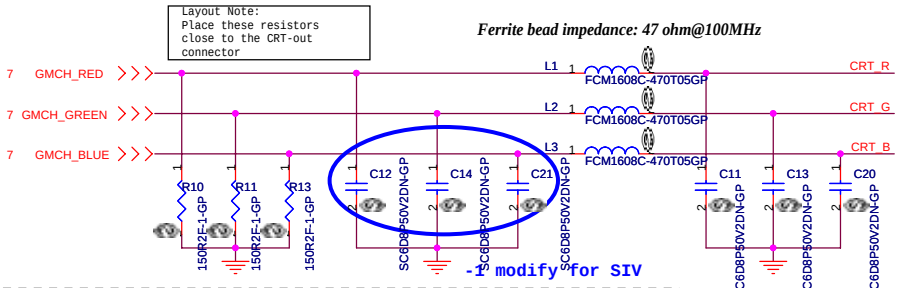
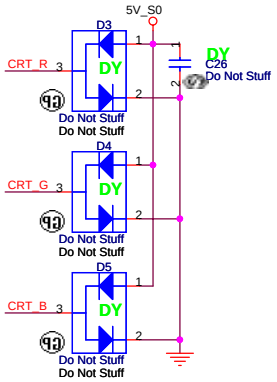
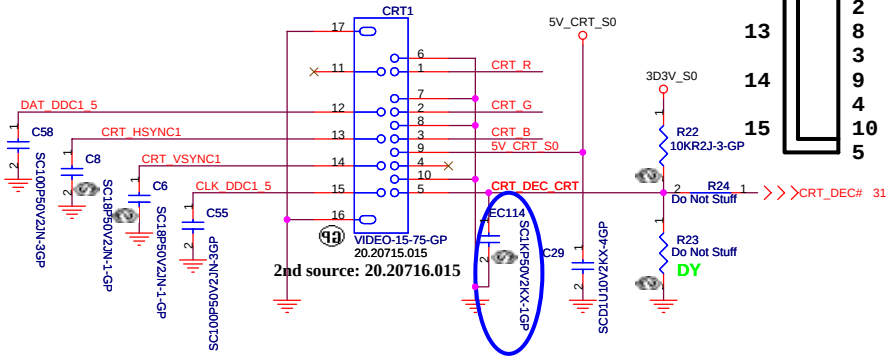
CRT I/F & CONNECTOR

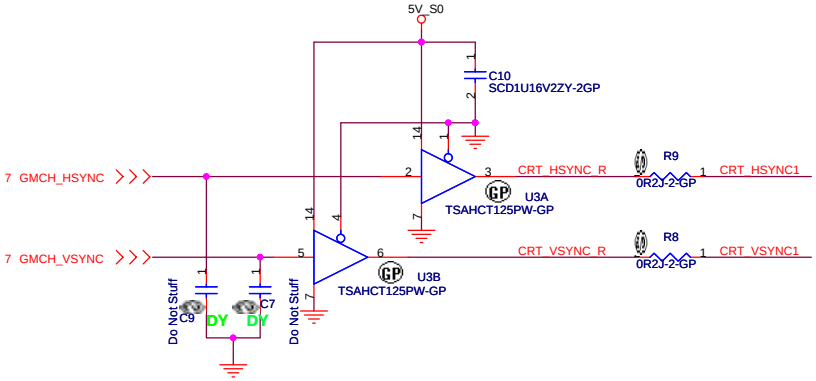




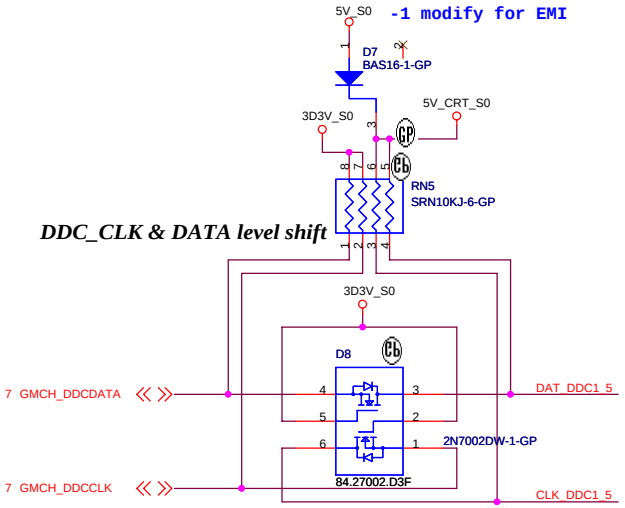


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

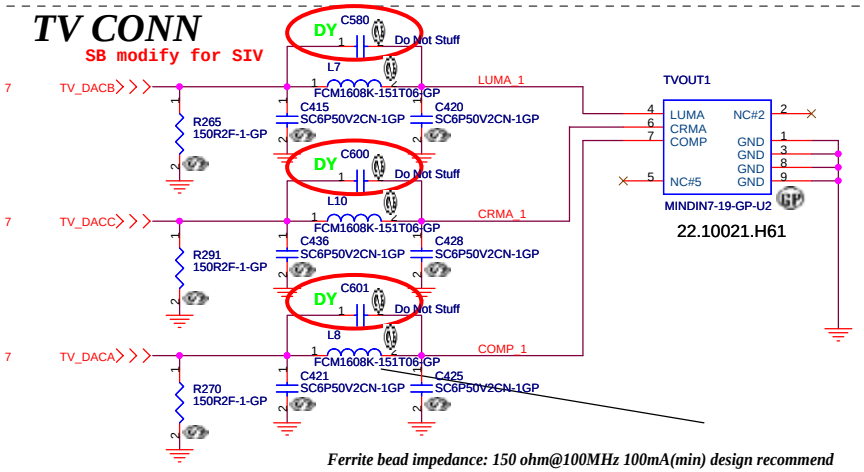


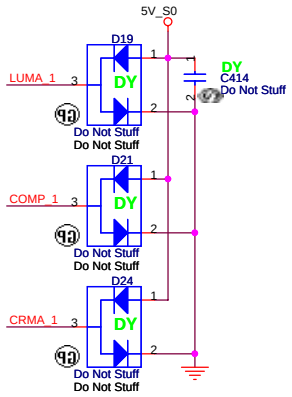
DDC_CLK & DATA level shift



TV CONN

SB modify for SIV





Ferrite bead impedance: 150 ohm@100MHz 100mA(min) design recommend

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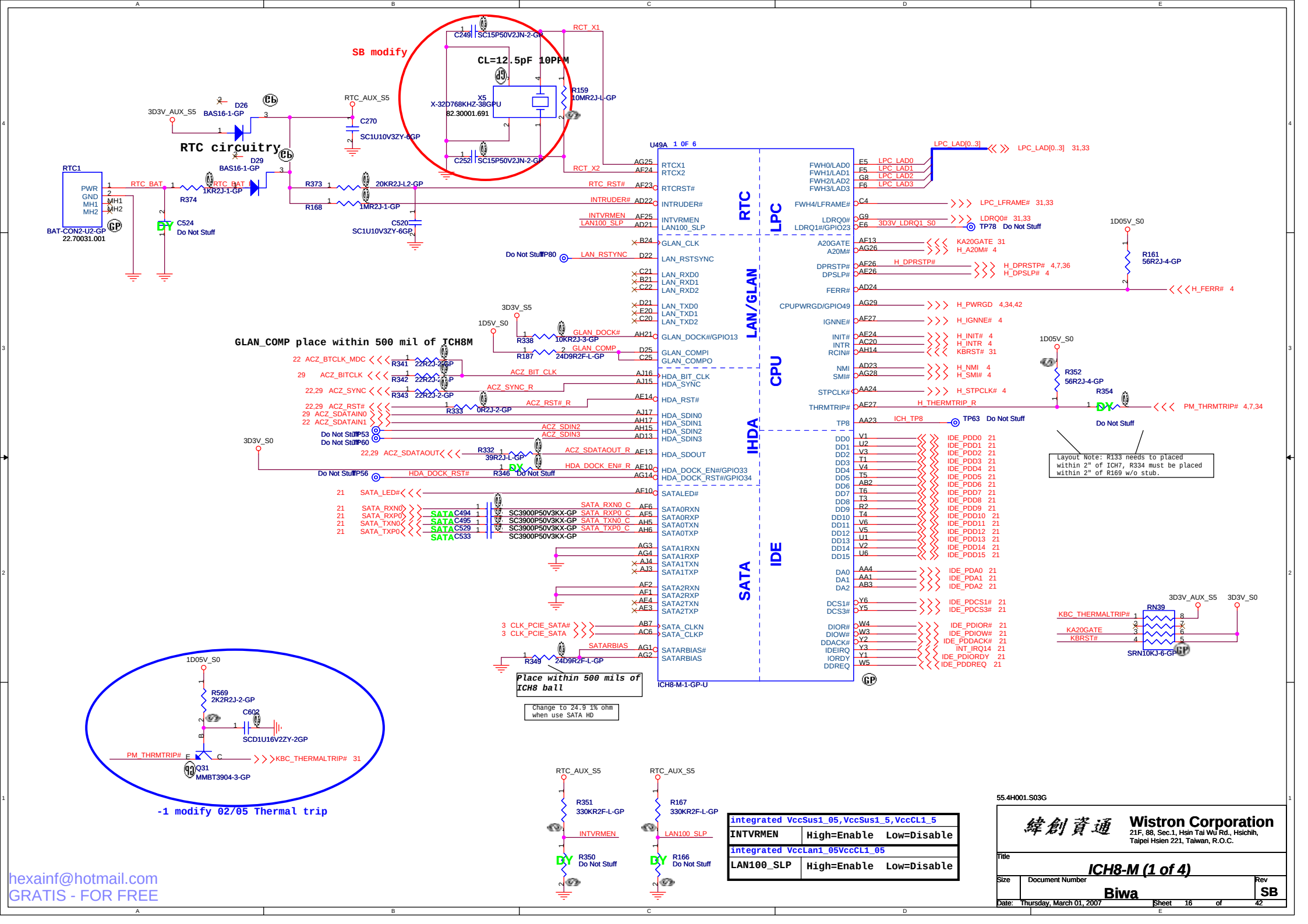
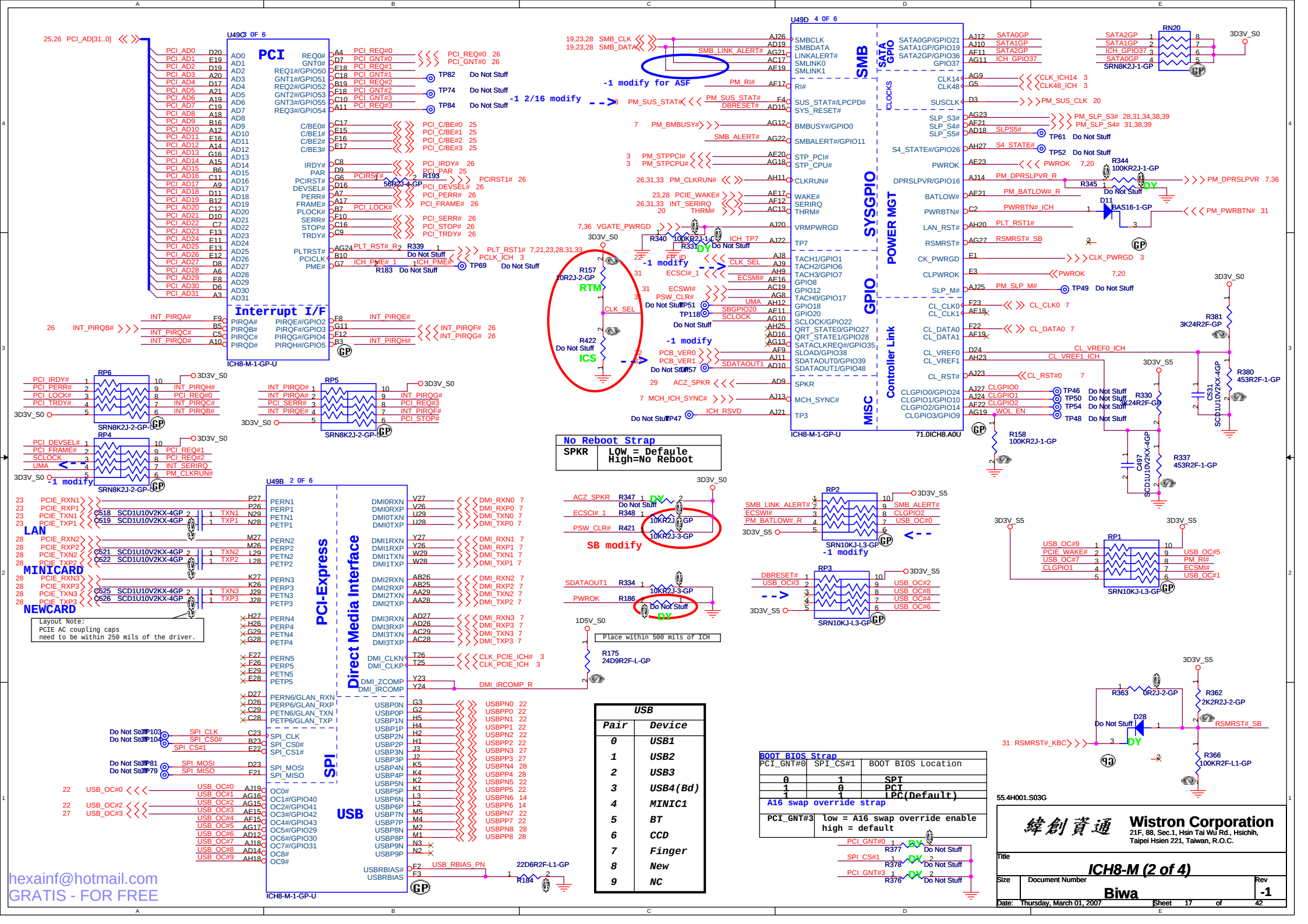
Title	CRT/TV Connector	
Size	Document Number: Biwa	Rev: -1
Date: Thursday, March 01, 2007	Sheet 15 of 42	




PCI
Interrupt I/F
ICH8-M-1-GP-U
SMB
SYSGPIO
GPIO
MISC
POWER MGT
Controller Link
SATA GPIO
CLOCKS
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINICARD
NEWCARD
-1 modify for ASF
-1 2/16 modify
-1 modify
SB modify
RTM
ICS
No Reboot Strap
SPKR LOW = Defaule High=No Reboot
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable high = default
USB
Pair Device
0 USB1
1 USB2
2 USB3
3 USB4(Bd)
4 MINIC1
5 BT
6 CCD
7 Finger
8 New
9 NC
Wistron Corporation
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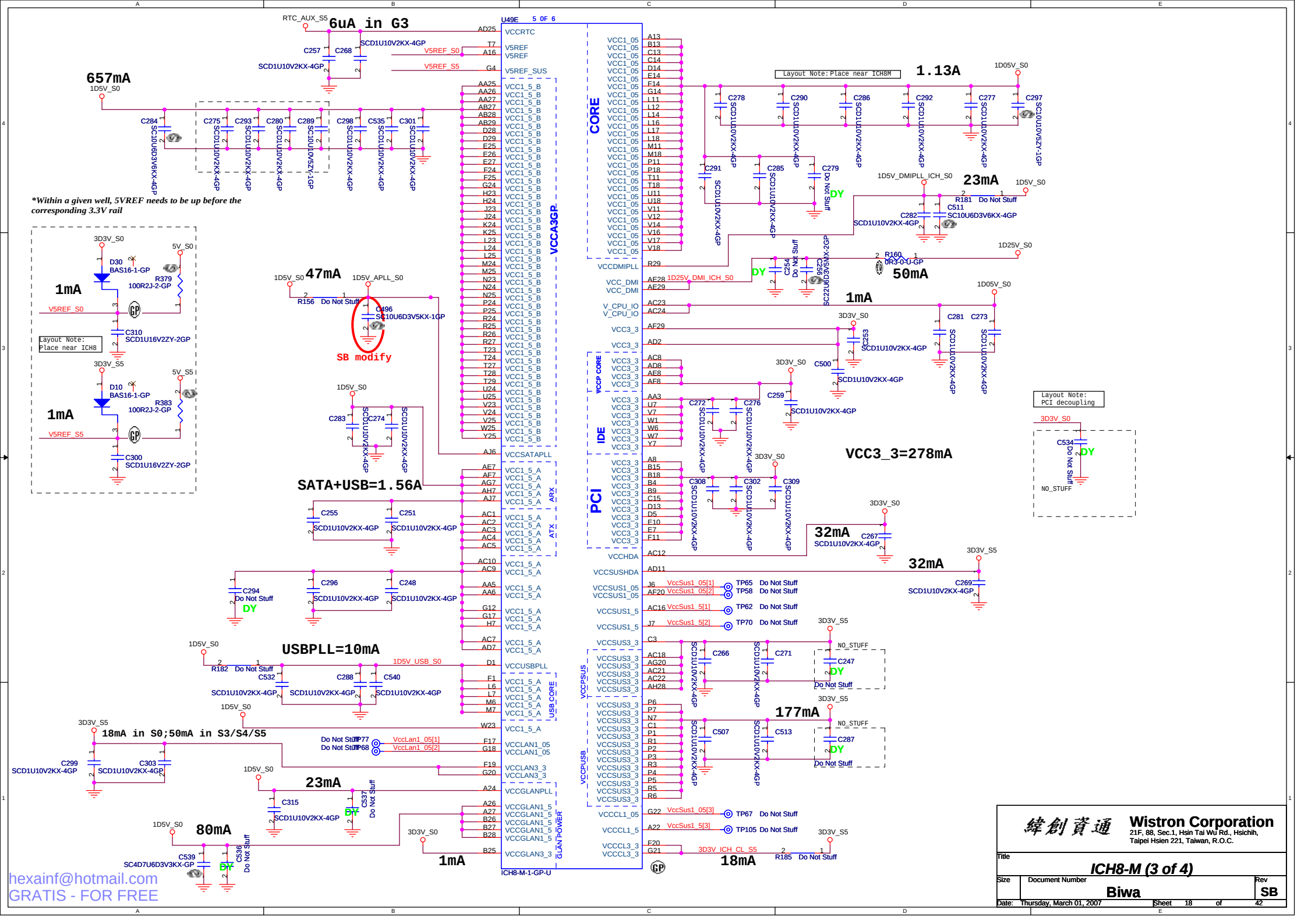
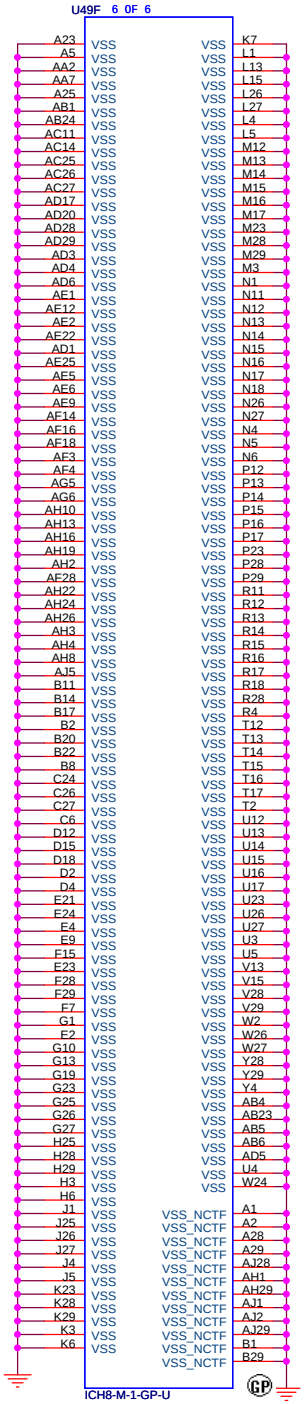
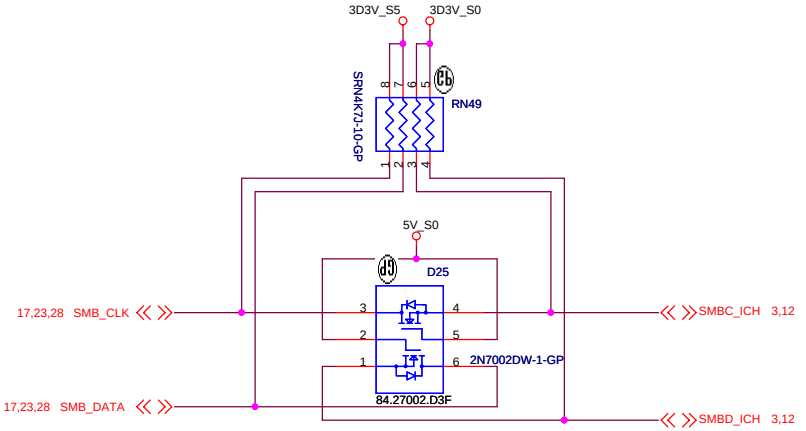
ICH8-M (2 of 4)
Biwa
Thursday, March 01, 2007
hexainf@hotmail.com
GRATIS - FOR FREE


6uA in G3
657mA
1.13A
23mA
47mA
1mA
50mA
SB modify
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
1mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH8
Layout Note: Place near ICH8M
Layout Note: PCI decoupling
NO_STUFF
U49E 5 OF 6
ICH8-M-1-GP-U
CORE
VCCA3GP
PCI
IDE
ATX
ARX
USB CORE
GLAN POWER
VCCPSUS
VCCPUSB
VCCP CORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8-M (3 of 4)
Biwa
SB
Thursday, March 01, 2007
Sheet 18 of 42
hexainf@hotmail.com
GRATIS - FOR FREE





D55 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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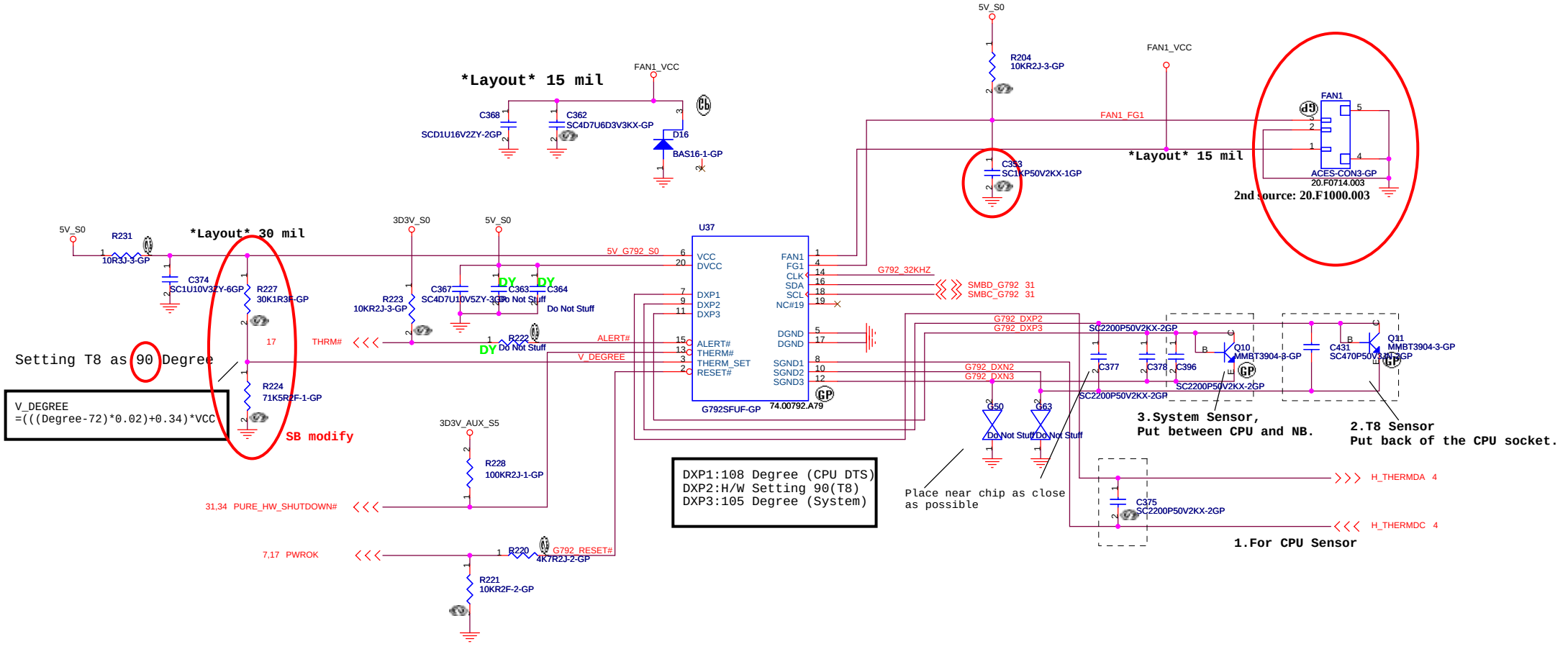
Title	ICH8-M (4 of 4)	
Size	Document Number: Biwa	Rev: SA
Date: Thursday, March 01, 2007	Sheet 19 of 42	



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

Biwa Thermal Table 1106

		T6	T7
Sencor 0	CPU DTS	100	102
Sencor 1	CPU G792 Analog	110	113
Sencor 2	System G792	85	87
Sencor 3	T8		
Sencor 4	ADIA status		

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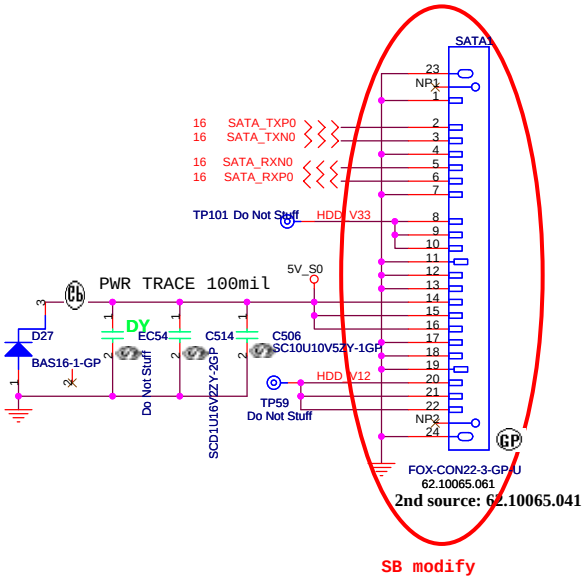
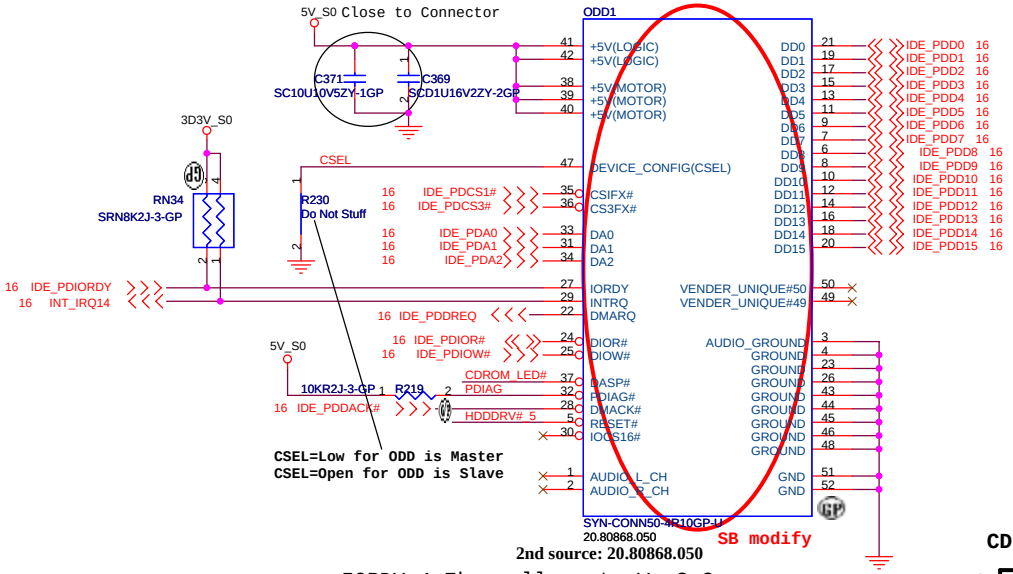
Title: Thermal/Fan Controllor
Size | Document Number: Biwa | Rev: SB
Date: Thursday, March 01, 2007 | Sheet 20 of 42

SATA Connector



SB modify

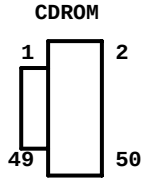
ODD Connector

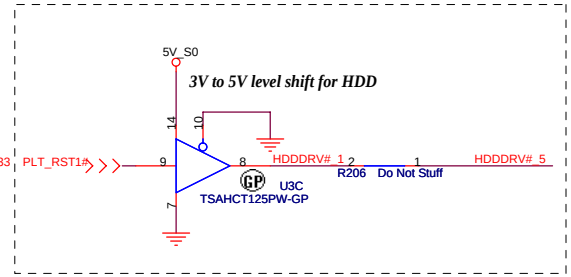


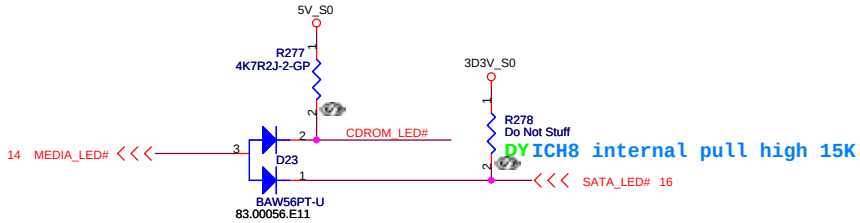
SB modify

CSEL=Low for ODD is Master
CSEL=Open for ODD is Slave

IORDY 4.7k pull-up to Vcc3_3
IDEIRQ 8.2k to 10k pull-up to Vcc3_3







ICH8 internal pull high 15K

55.4H001.S03G

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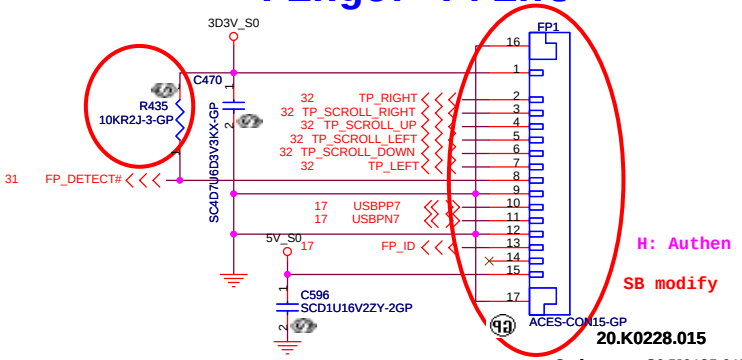
Title: HDD and CDROM

Size	Document Number	Rev
	Biwa	SB

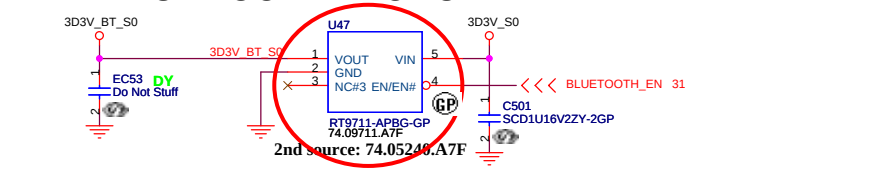
Date: Thursday, March 01, 2007 Sheet 21 of 42

Finger Print



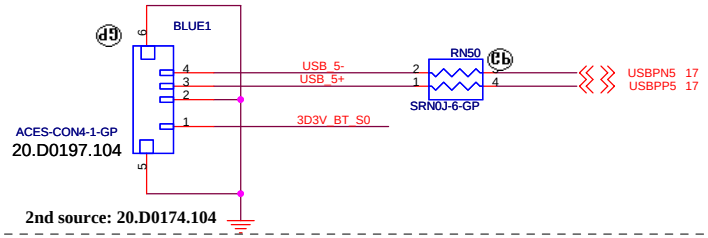
2nd source: 20.K0185.015

BLUETOOTH MODULE



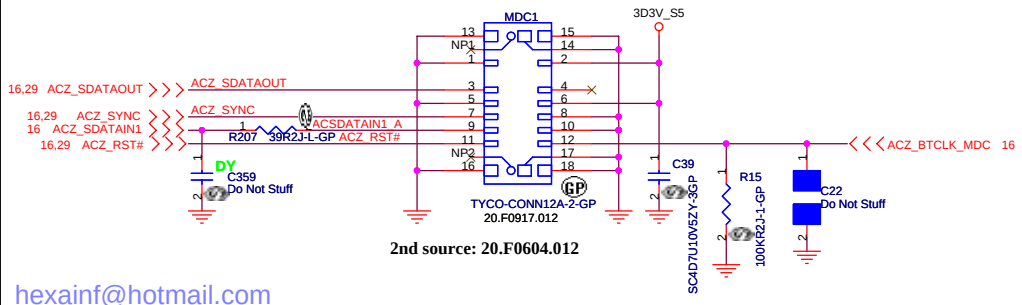
2nd source: 74.05240.A7F

EC21 put near BLUE1 / all USB put one choke near connector by EMI request

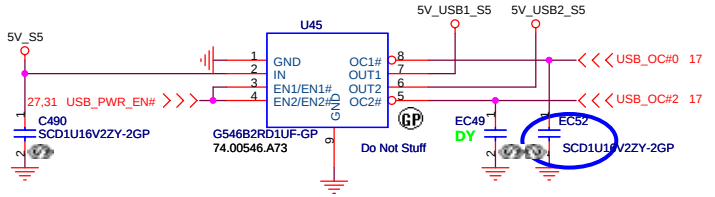


2nd source: 20.D0174.104

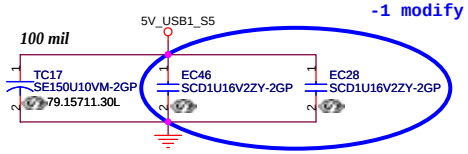
MDC 1.5 CONN

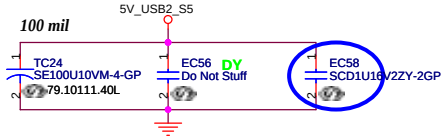


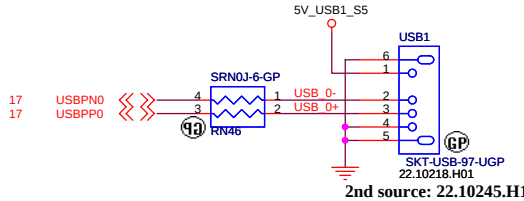
2nd source: 20.F0604.012



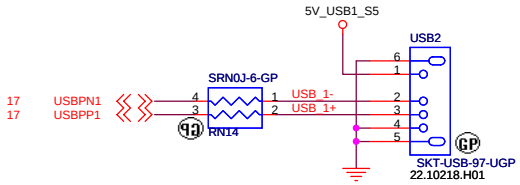
-1 modify for EMC



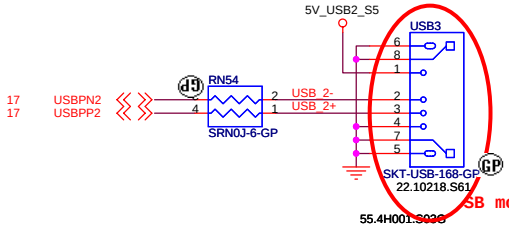




2nd source: 22.10245.H11



2nd source: 22.10245.H11



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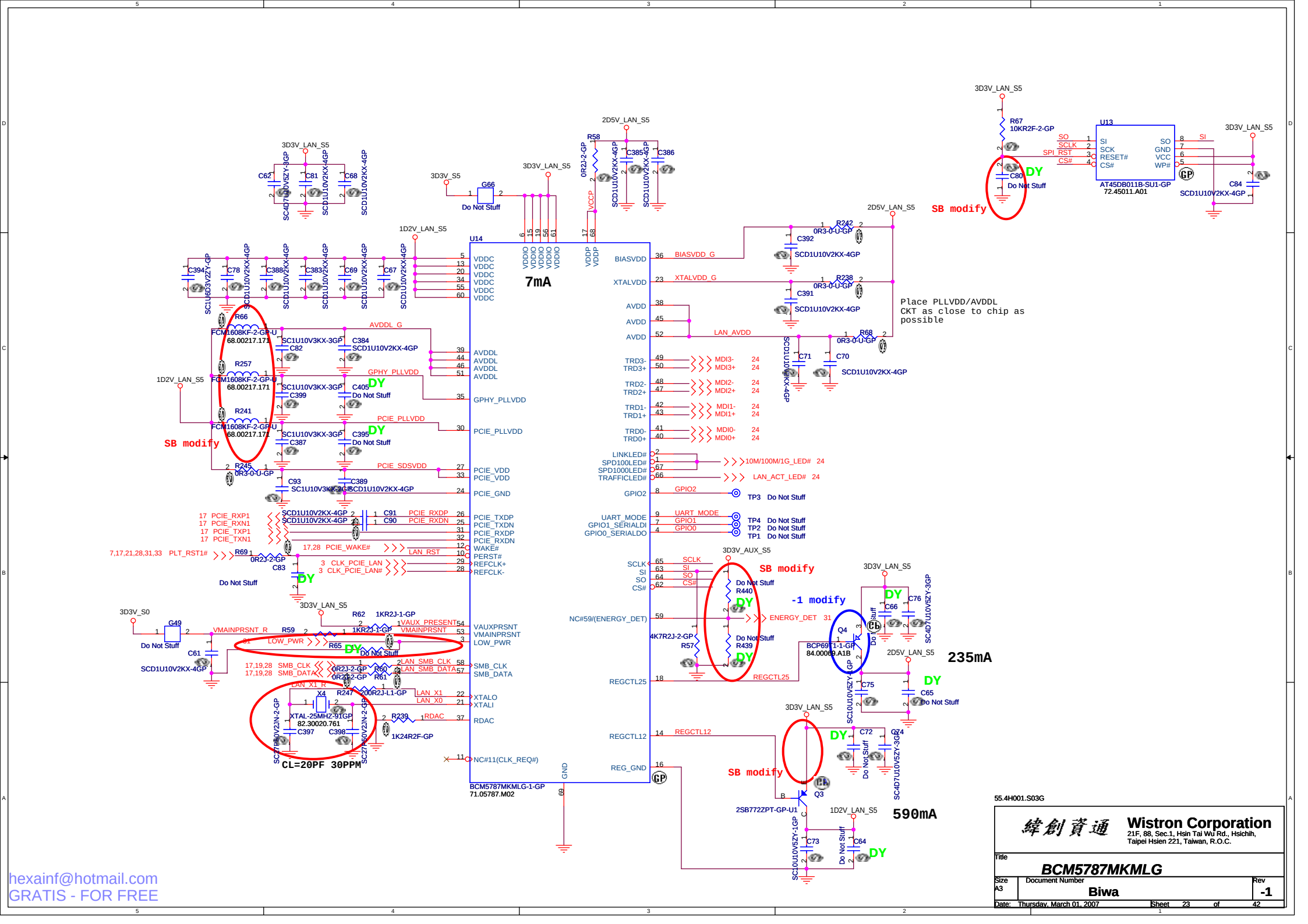
Title: **USB / MDC / BLUETOOTH / FP**

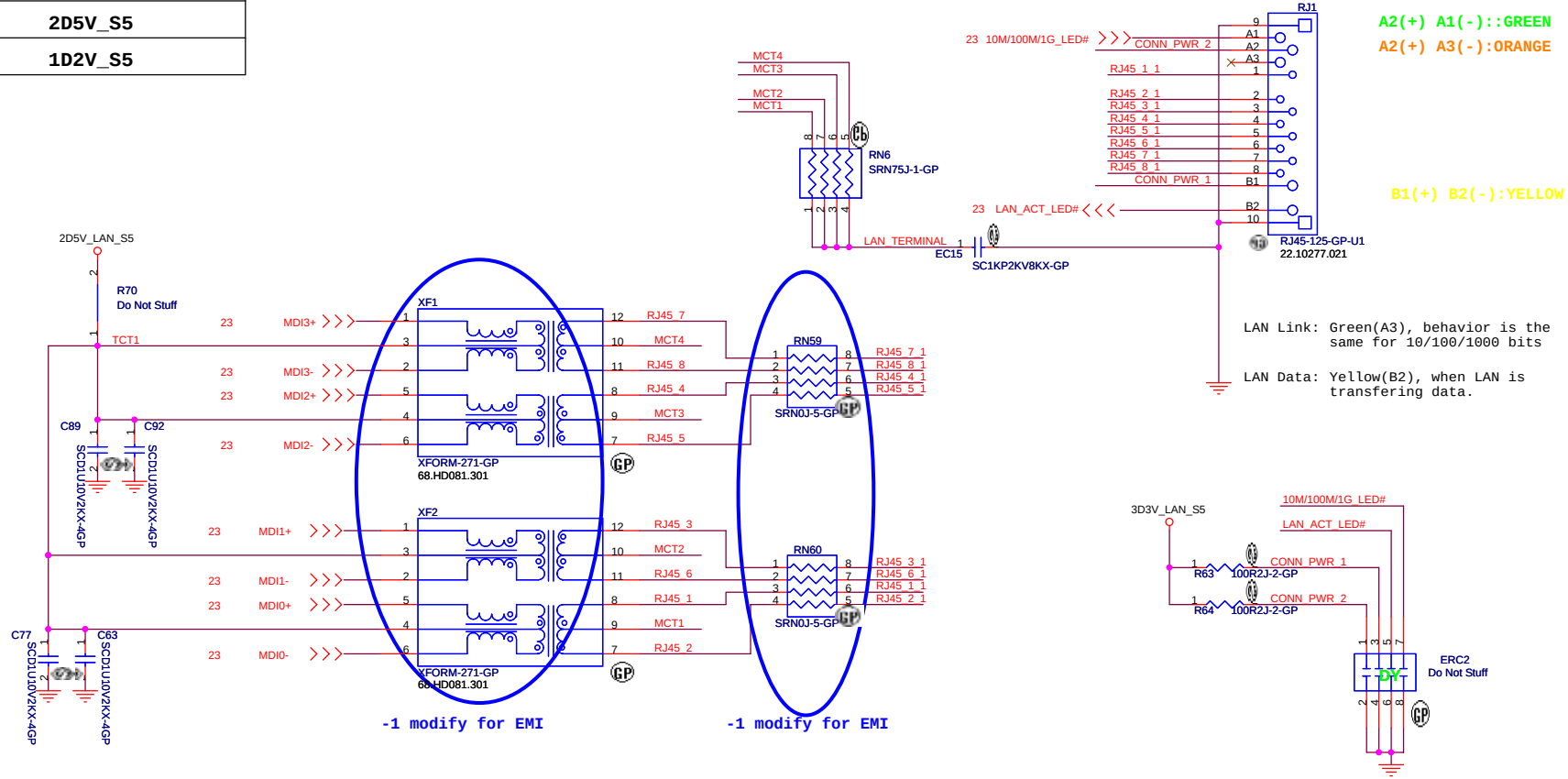
Size	Document Number	Rev
	Biwa	-1

Date: Thursday, March 01, 2007 Sheet 22 of 42



Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

55.4H001.S03G

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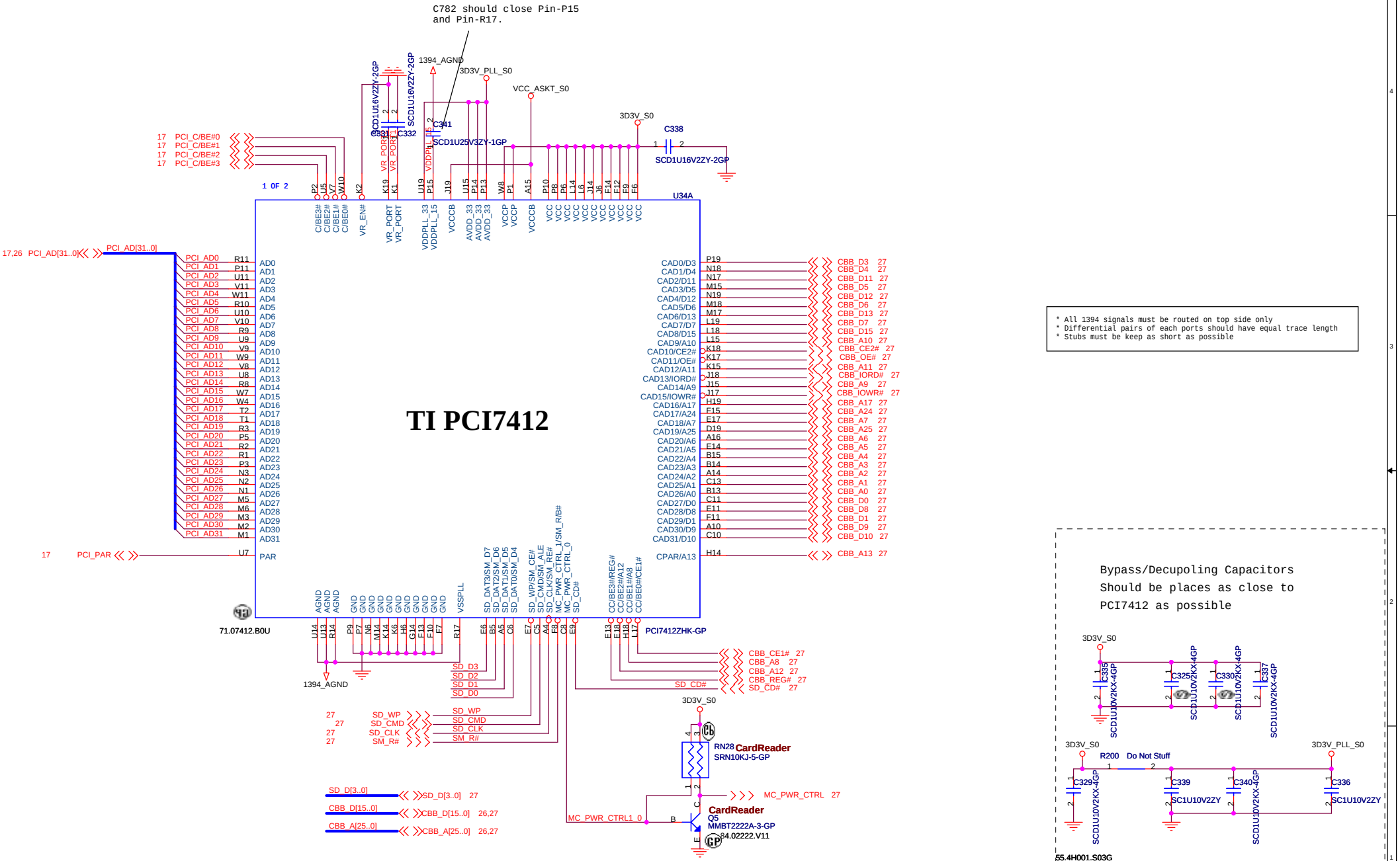
Title: **LAN Connector**

Size	Document Number	Rev
A3	Biwa	-1

Date: Thursday, March 01, 2007 Sheet 24 of 42



緯創資通	**Wistron Corporation**
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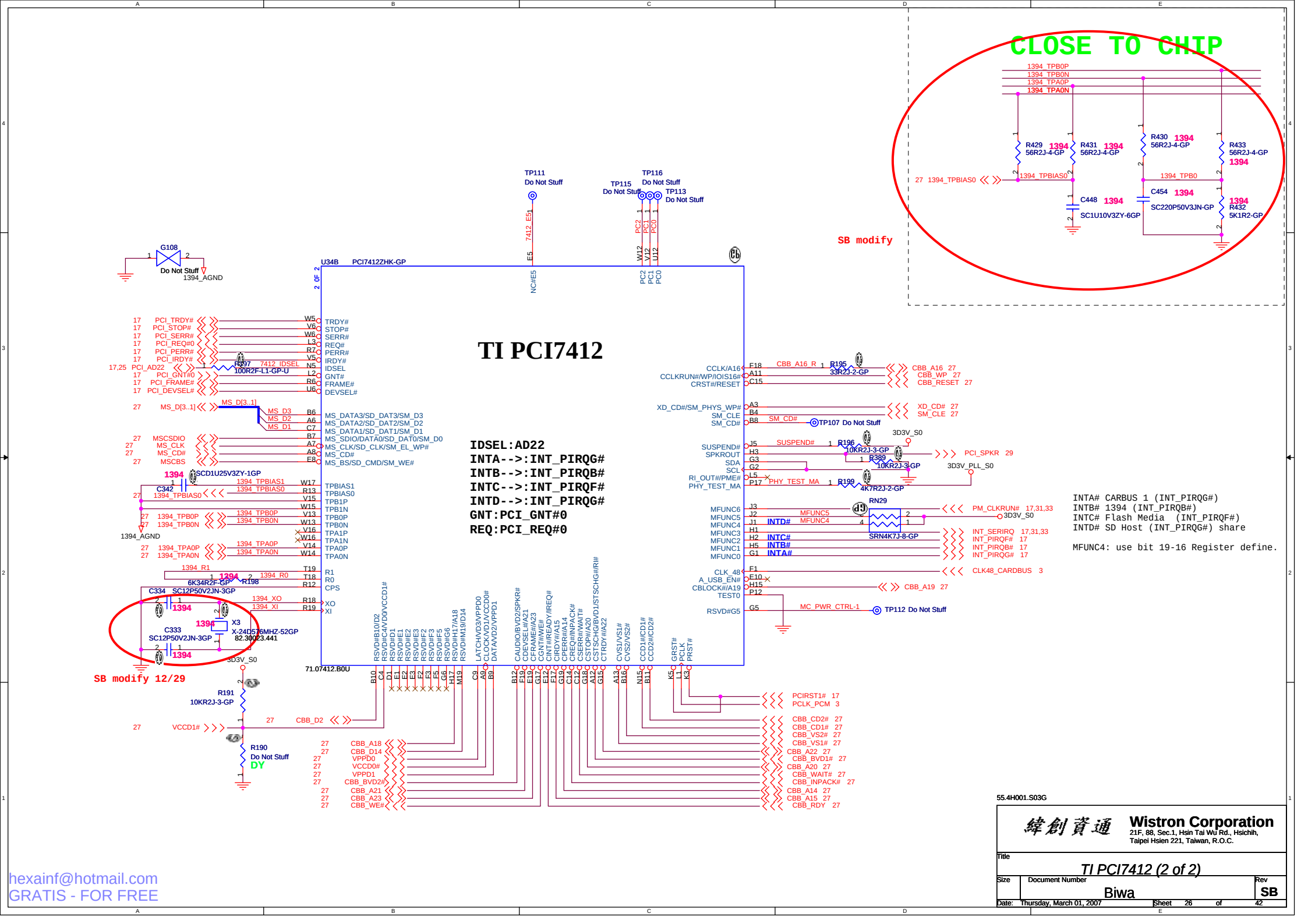
Title	*TI PCI7412 (1 of 2)*
Size	Document Number: Biwa
Rev	SA
Date: Thursday, March 01, 2007	Sheet 25 of 42


CLOSE TO CHIP
1394_TPB0P
1394_TPB0N
1394_TPA0P
1394_TPA0N
R429 1394 56R2J-4-GP
R431 1394 56R2J-4-GP
R430 1394 56R2J-4-GP
R433 56R2J-4-GP 1394
27 1394_TPBIAS0
1394_TPBIAS0
1394_TPB0
C448 1394 SC1U10V3ZY-6GP
C454 1394 SC220P50V3JN-GP
R432 5K1R2-GP 1394
SB modify
TP111 Do Not Stuff
TP115 Do Not Stuff
TP116 Do Not Stuff
TP113 Do Not Stuff
7412_E51
PC2 PC1 PC0
W12 V12 U12
NC#E5
G108
Do Not Stuff
1394_AGND
U34B PCI7412ZHK-GP
2 OF 2
TI PCI7412
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQB#
INTC-->:INT_PIRQF#
INTD-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
TRDY# STOP# SERR# REQ# PERR# IRDY# IDSEL GNT# FRAME# DEVSEL#
PCI_TRDY# PCI_STOP# PCI_SERR# PCI_REQ#0 PCI_PERR# PCI_IRDY#
PCI_AD22 PCI_GNT#0 PCI_FRAME# PCI_DEVSEL#
R197 7412_IDSEL 100R2F-L1-GP-U
MS_D[3..1]
MS_DATA3/SD_DAT3/SM_D3
MS_DATA2/SD_DAT2/SM_D2
MS_DATA1/SD_DAT1/SM_D1
MS_SDIO/DATA0/SD_DAT0/SM_D0
MS_CLK/SD_CLK/SM_EL_WP#
MS_CD#
MS_BS/SD_CMD/SM_WE#
MSCSDIO MS_CLK MS_CD# MSCBS
SCD1U25V3ZY-1GP
C342
1394_TPBIAS1 1394_TPBIAS0
TPBIAS1 TPBIAS0 TPB1P TPB1N TPB0P TPB0N TPA1P TPA1N TPA0P TPA0N
1394_TPB0P 1394_TPB0N
1394_TPA0P 1394_TPA0N
1394_R1 1394_R0
R198 6K34R2F-GP
R1 R0 CPS
C334 SC12P50V2JN-3GP
1394_XO 1394_XI
XO XI
X3 X-24D576MHZ-52GP 82.30023.441
C333 SC12P50V2JN-3GP
3D3V_S0
SB modify 12/29
R191 10KR2J-3-GP
R190 Do Not Stuff DY
VCCD1#
CBB_D2
71.07412.B0U
RSVD#B10/D2 RSVD#C4/VD0/VCCD1# RSVD#D1 RSVD#E1 RSVD#E2 RSVD#E3 RSVD#F2 RSVD#F3 RSVD#F5 RSVD#G6 RSVD#H17/A18 RSVD#M19/D14
LATCH/VD3/VPPD0 CLOCK/VD1/VCCD0# DATA/VD2/VPPD1
CAUDIO/BVD2/SPKR# CDEVSEL#/A21 CFRAME#/A23 CGNT#/WE# CINT#/READY/IREQ# CIRDY#/A15 CPERR#/A14 CREQ#/INPACK# CSERR#/WAIT# CSTOP#/A20 CSTSCHG/BVD1/STSCHG#/RI# CTRDY#/A22
CVS1/VS1# CVS2/VS2#
CCD1#/CD1# CCD2#/CD2#
GRST# PCLK PRST#
PCIRST1# 17
PCLK_PCM 3
CBB_CD2# 27
CBB_CD1# 27
CBB_VS2# 27
CBB_VS1# 27
CBB_A22 27
CBB_BVD1# 27
CBB_A20 27
CBB_WAIT# 27
CBB_INPACK# 27
CBB_A14 27
CBB_A15 27
CBB_RDY 27
CBB_A18 27
CBB_D14 27
VPPD0 27
VCCD0# 27
VPPD1 27
CBB_BVD2# 27
CBB_A21 27
CBB_A23 27
CBB_WE# 27
CCLK/A16 CCLKRUN#/WP/IOIS16# CRST#/RESET
CBB_A16_R R195 33R2J-2-GP
CBB_A16 27 CBB_WP 27 CBB_RESET 27
XD_CD#/SM_PHYS_WP# SM_CLE SM_CD#
XD_CD# 27 SM_CLE 27
SM_CD# TP107 Do Not Stuff
SUSPEND# SPKROUT SDA SCL RI_OUT#/PME# PHY_TEST_MA
SUSPEND# R196 10KR2J-3-GP
PCI_SPKR 29
R389 10KR2J-3-GP
3D3V_PLL_S0
PHY_TEST_MA R199 4K7R2J-2-GP
RN29
MFUNC6 MFUNC5 MFUNC4 MFUNC3 MFUNC2 MFUNC1 MFUNC0
INTD# INTC# INTB# INTA#
SRN4K7J-8-GP
PM_CLKRUN# 17,31,33
INT_SERIRQ 17,31,33
INT_PIRQF# 17
INT_PIRQB# 17
INT_PIRQG# 17
CLK_48 A_USB_EN# CBLOCK#/A19 TEST0
CLK48_CARDBUS 3
CBB_A19 27
RSVD#G5
MC_PWR_CTRL-1
TP112 Do Not Stuff
INTA# CARBUS 1 (INT_PIRQG#)
INTB# 1394 (INT_PIRQB#)
INTC# Flash Media (INT_PIRQF#)
INTD# SD Host (INT_PIRQG#) share
MFUNC4: use bit 19-16 Register define.
55.4H001.S03G
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (2 of 2)
Size
Document Number
Biwa
Rev
SB
Date: Thursday, March 01, 2007
Sheet 26 of 42
hexainf@hotmail.com
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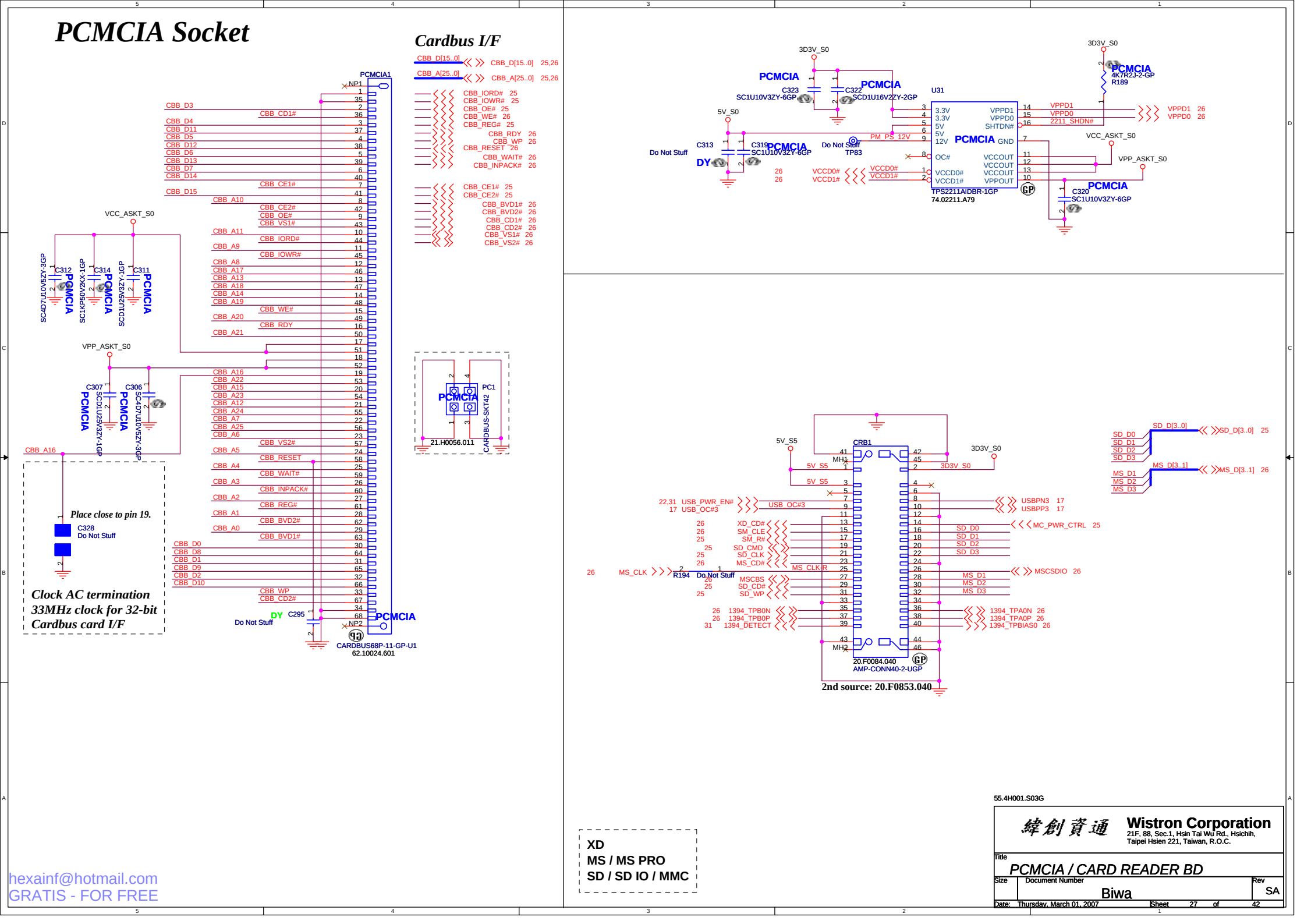
PCMCIA Socket



55.4H001.S03G

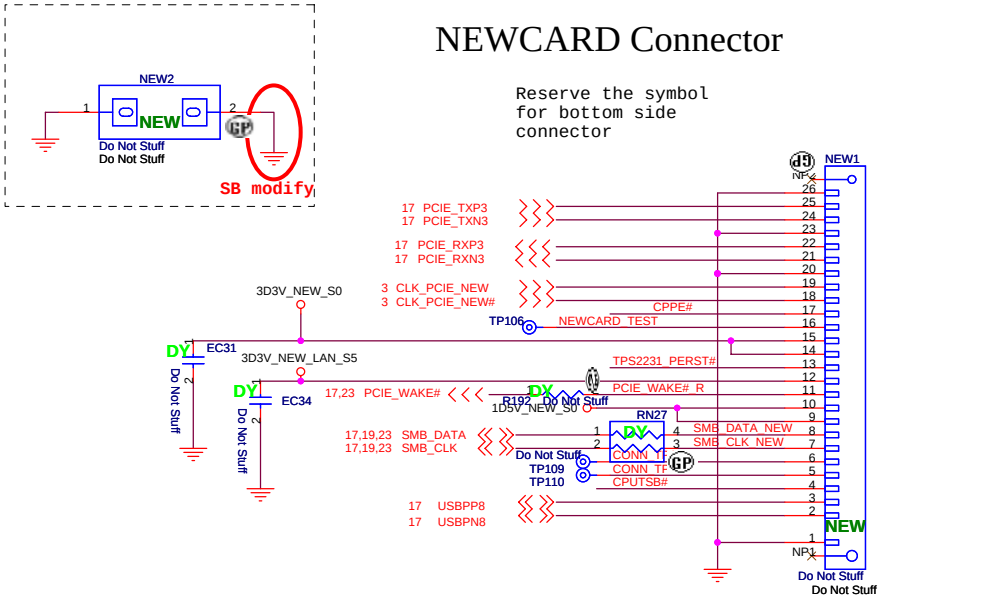
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / CARD READER BD

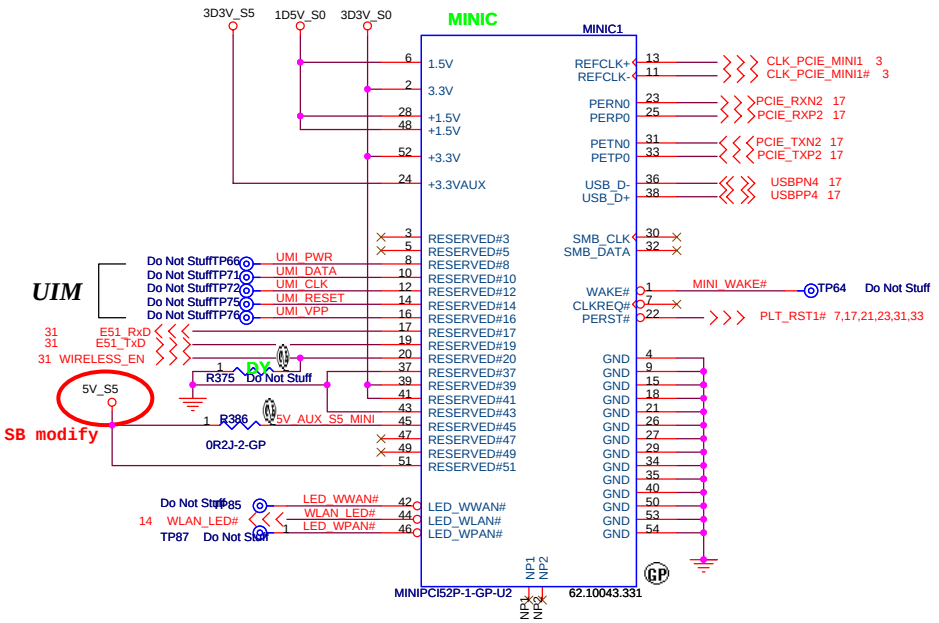
Size	Document Number	Rev
	Biwa	SA

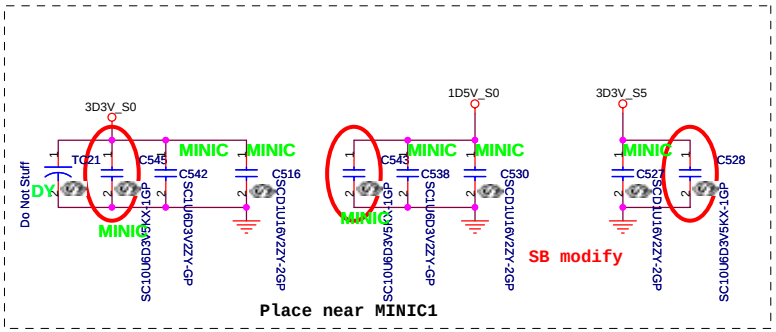
Date: Thursday, March 01, 2007 Sheet 27 of 42

NEWCARD Connector



Mini Card Connector





55.4H001.S03G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / NEW CARD

Size | Document Number: Biwa | Rev: SB

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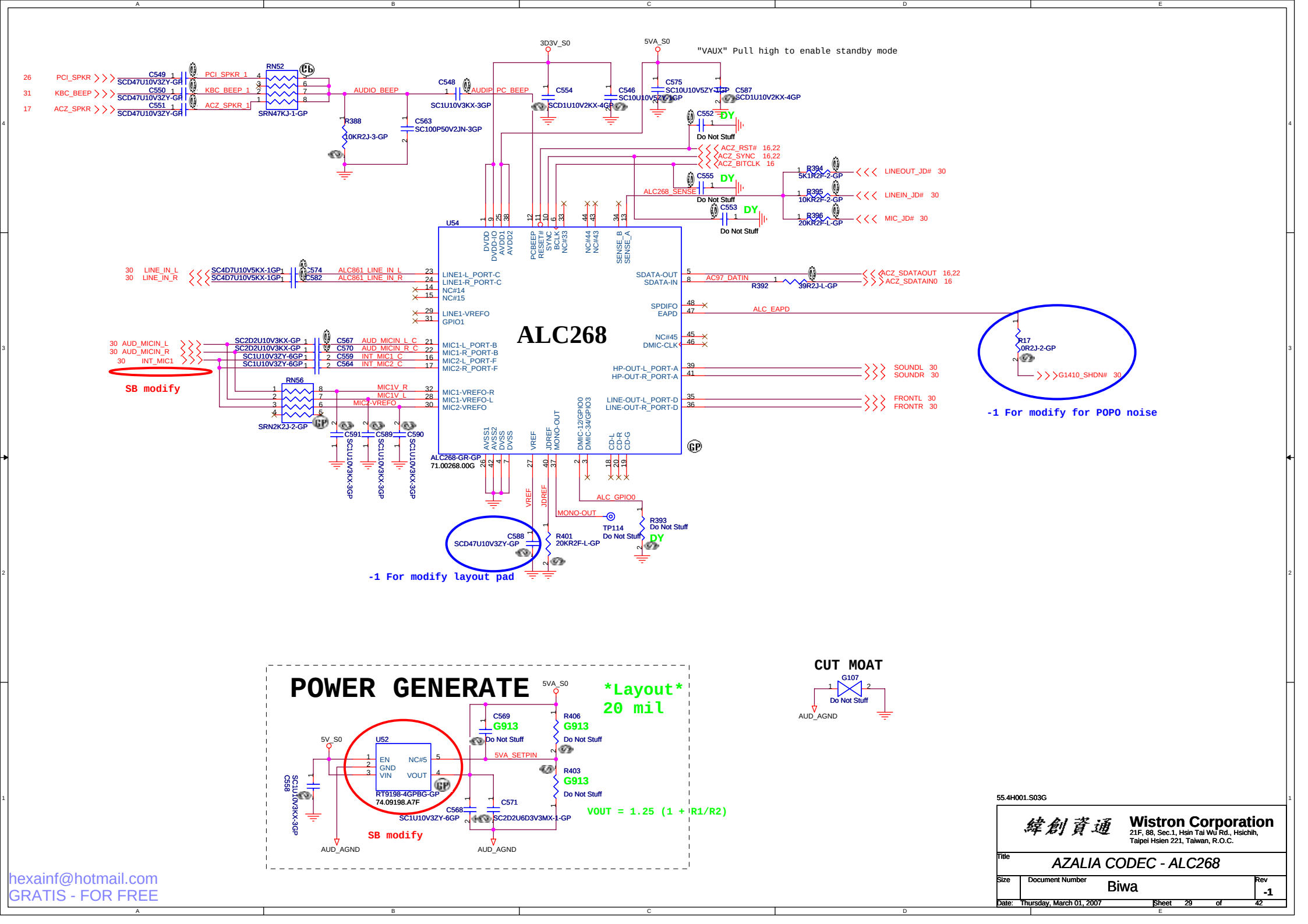

55.4H001.S03G

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - ALC268

Size | Document Number: Biwa | Rev: -1

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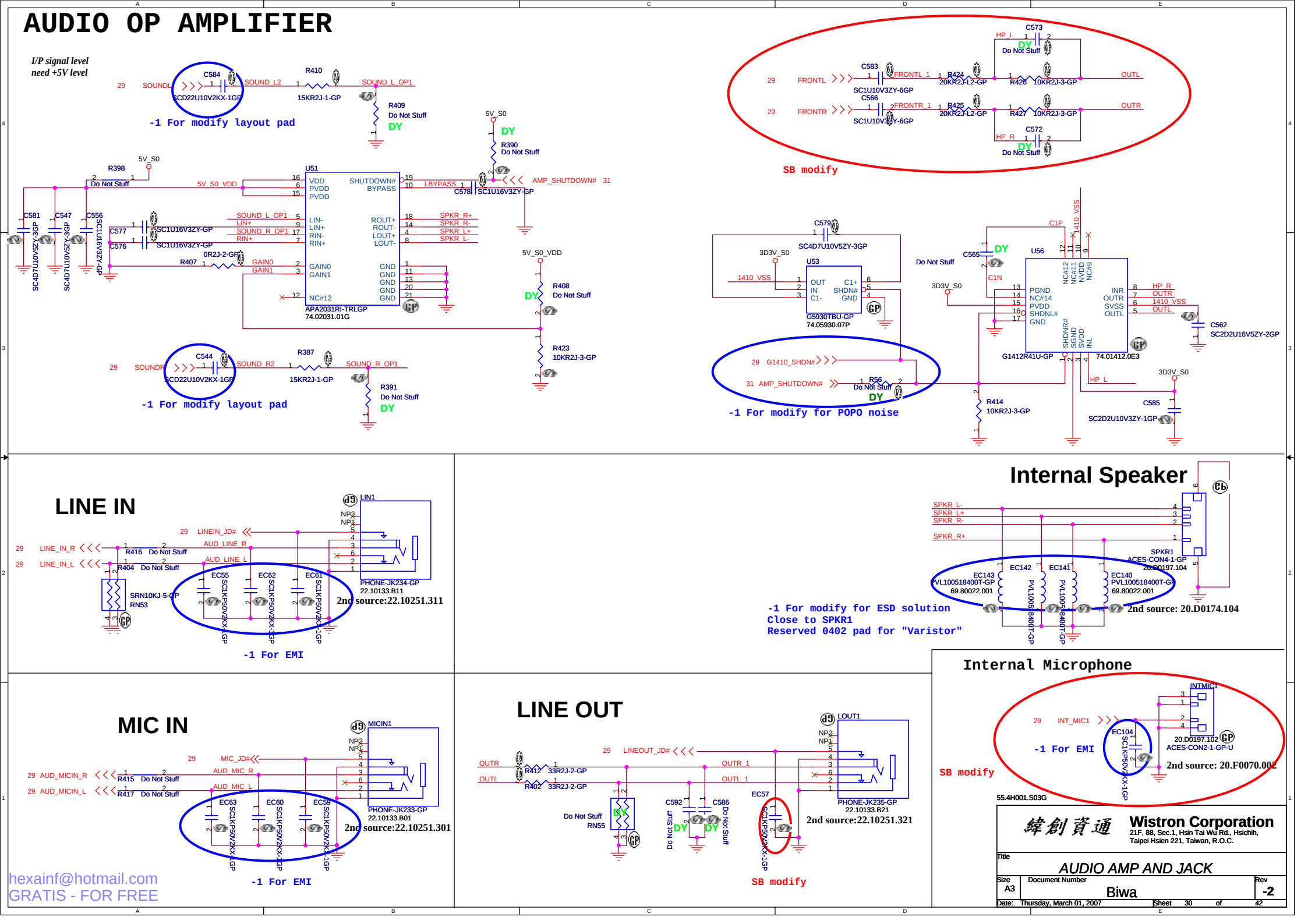
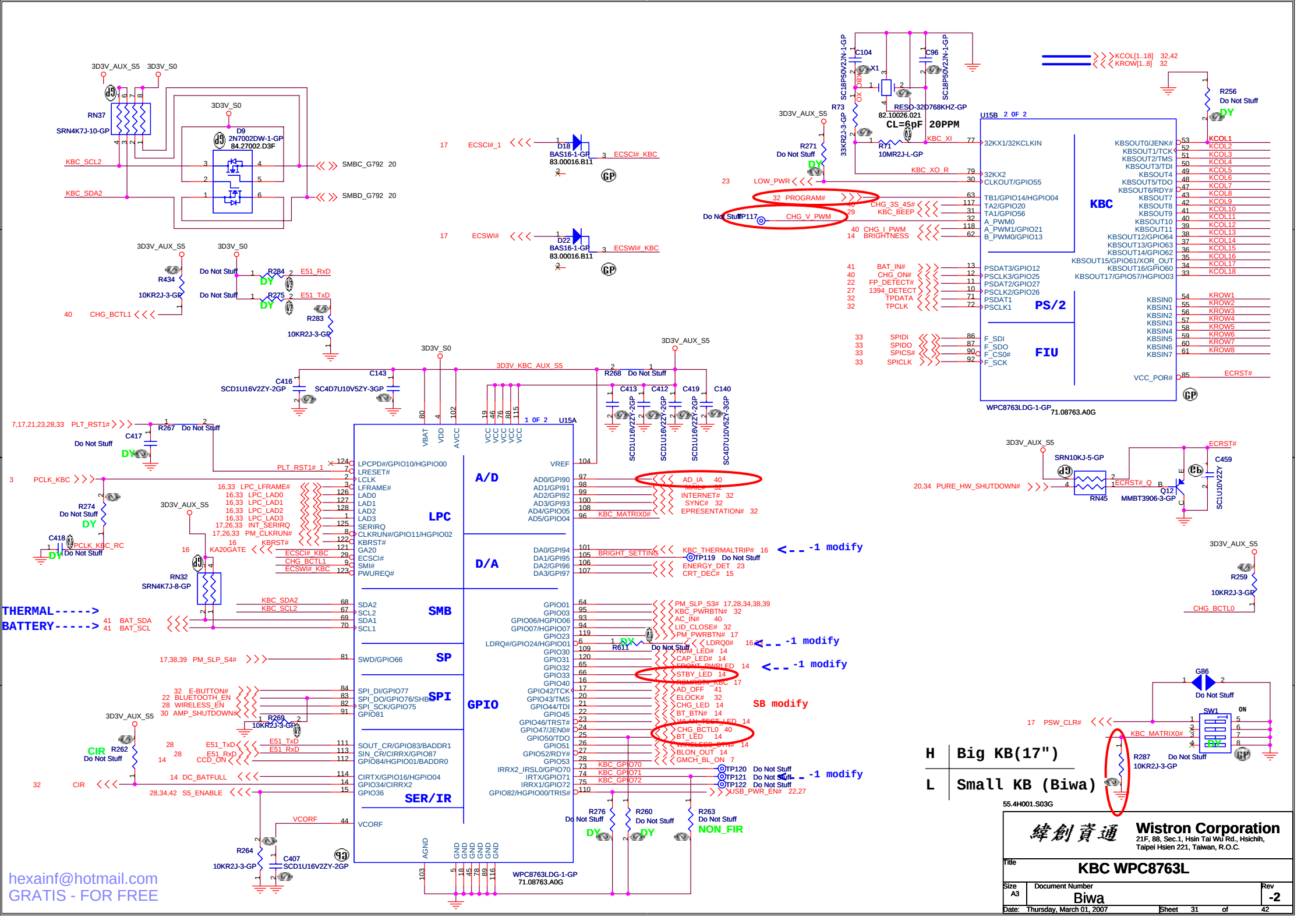
AUDIO OP AMPLIFIER




KBC
PS/2
FIU
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
WPC8763LDG-1-GP
71.08763.A0G
THERMAL - - - - ->
BATTERY - - - - ->
SB modify
-1 modify
NON_FIR
H | Big KB(17")
L | Small KB (Biwa)
55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8763L
Biwa
Thursday, March 01, 2007
hexainf@hotmail.com
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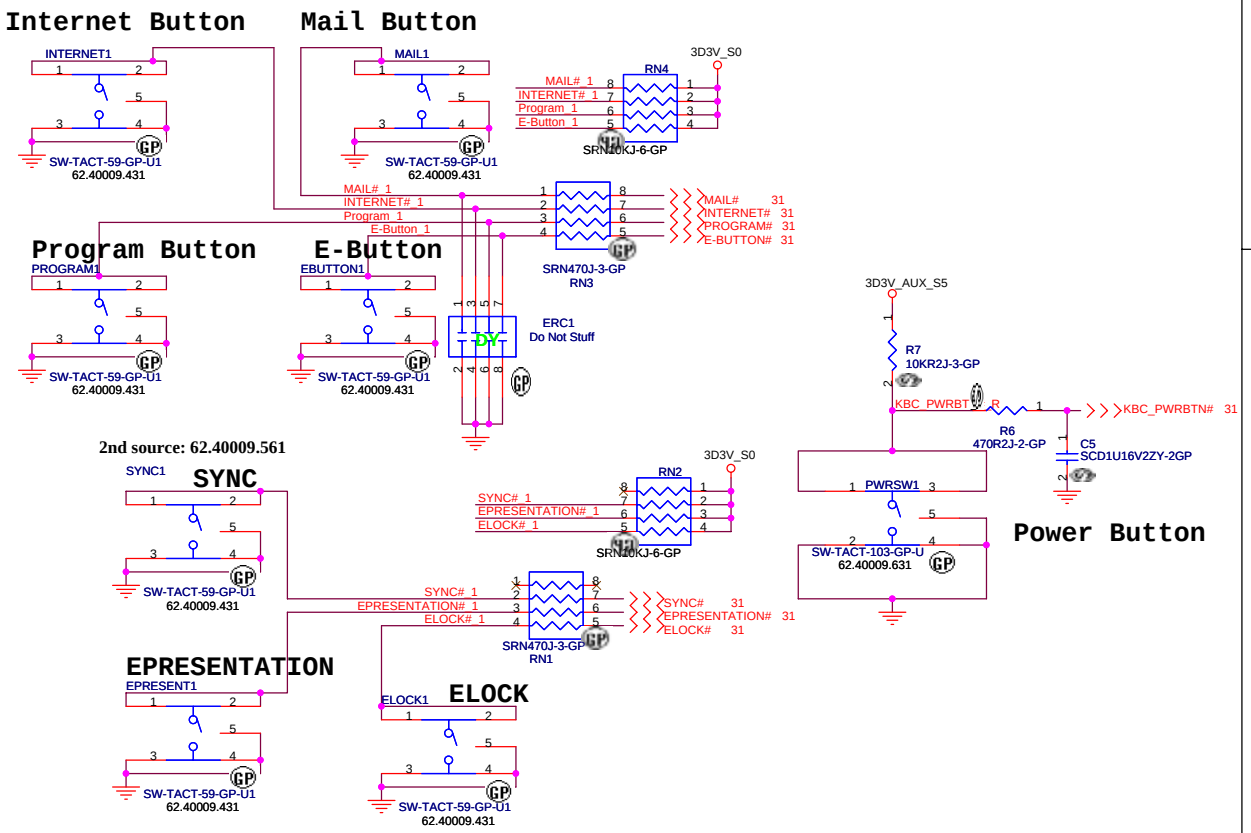

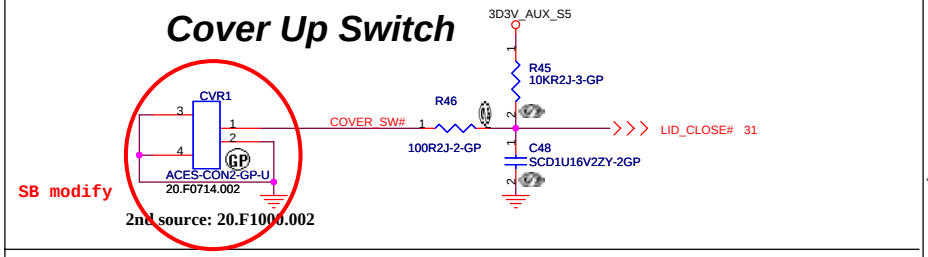

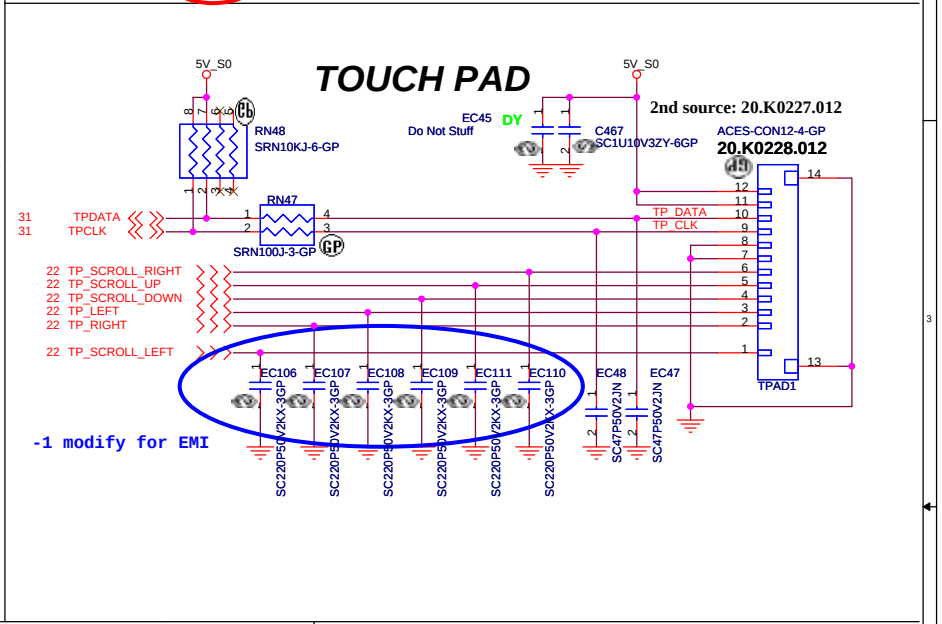

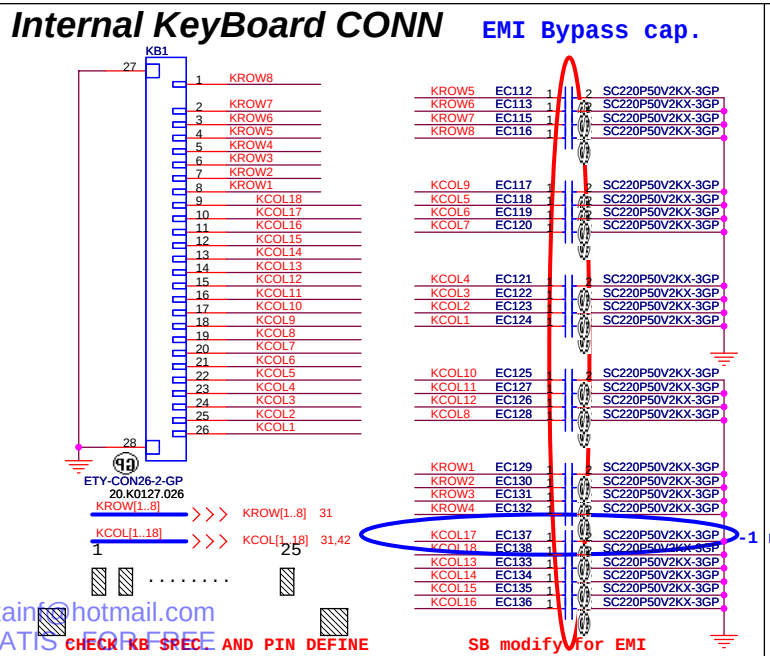

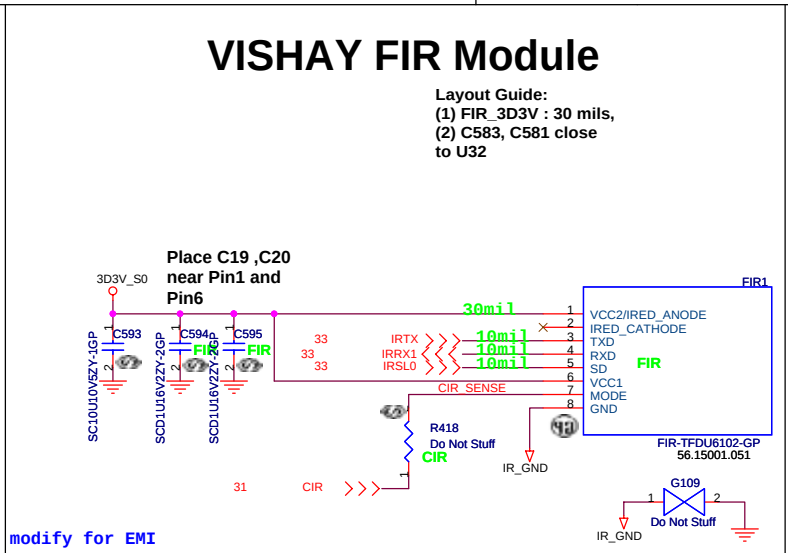

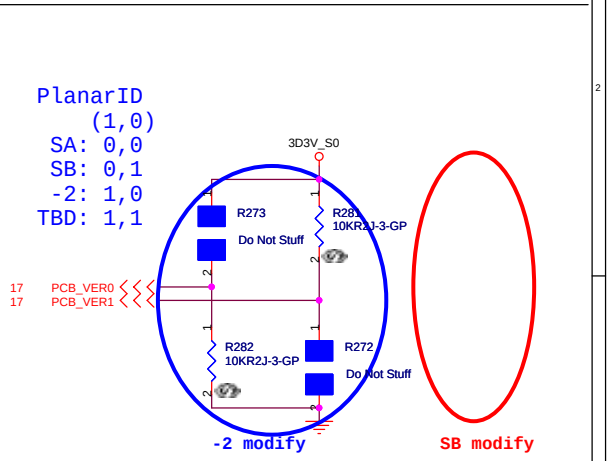

55.4H001.S03G

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD / FIR

Size | Document Number: Biwa | Rev: -2

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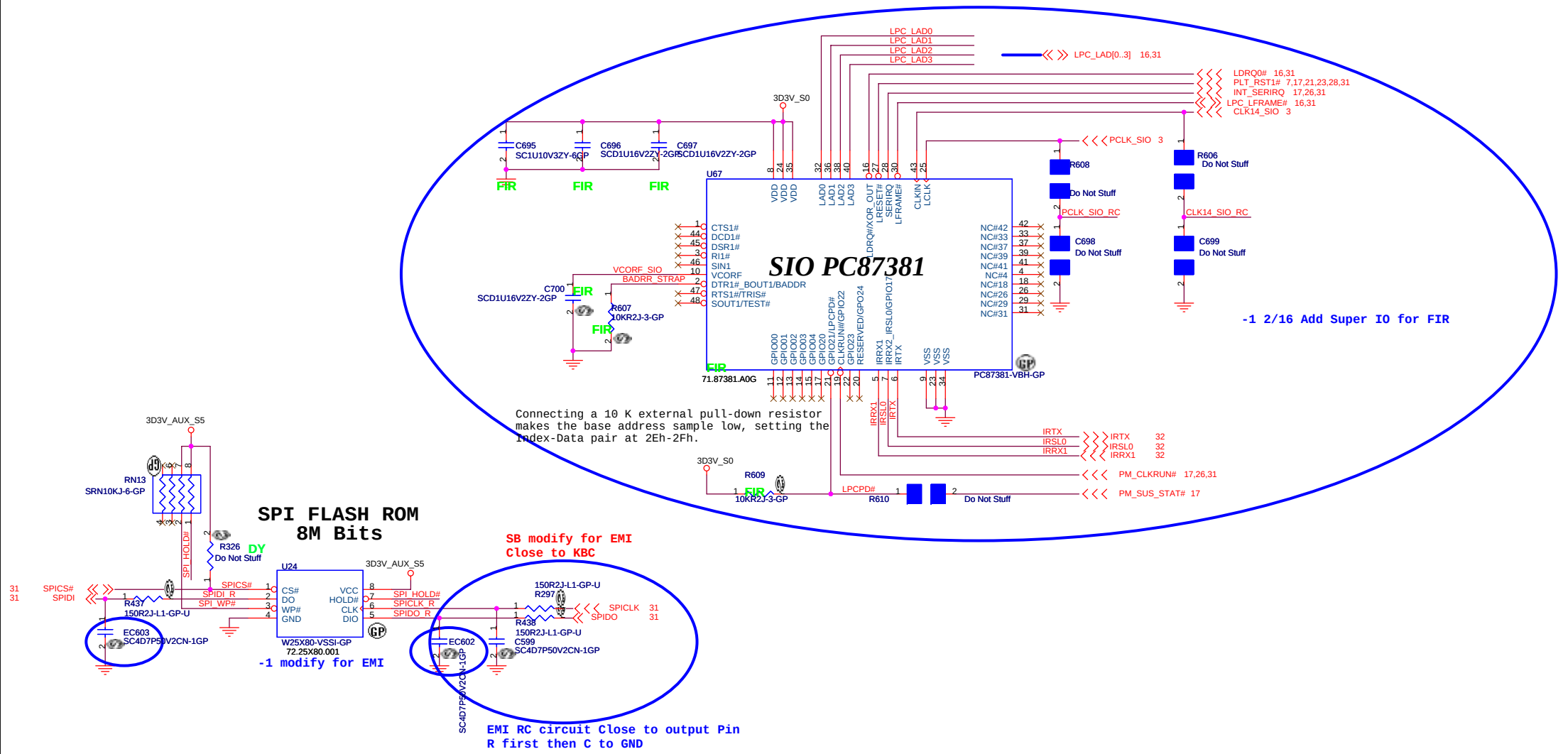


55.4H001.S03G

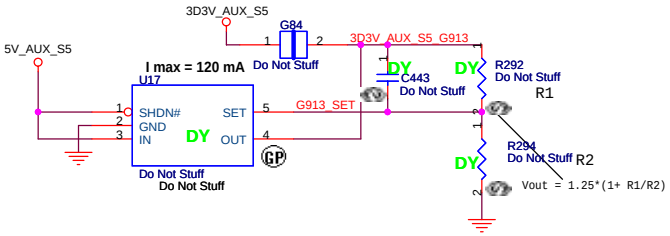
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

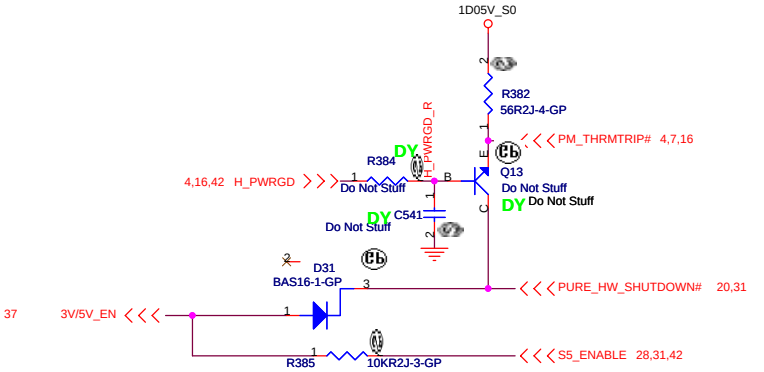
Title: BIOS & Super IO

Size	Document Number	Rev
A3	Biwa	-2

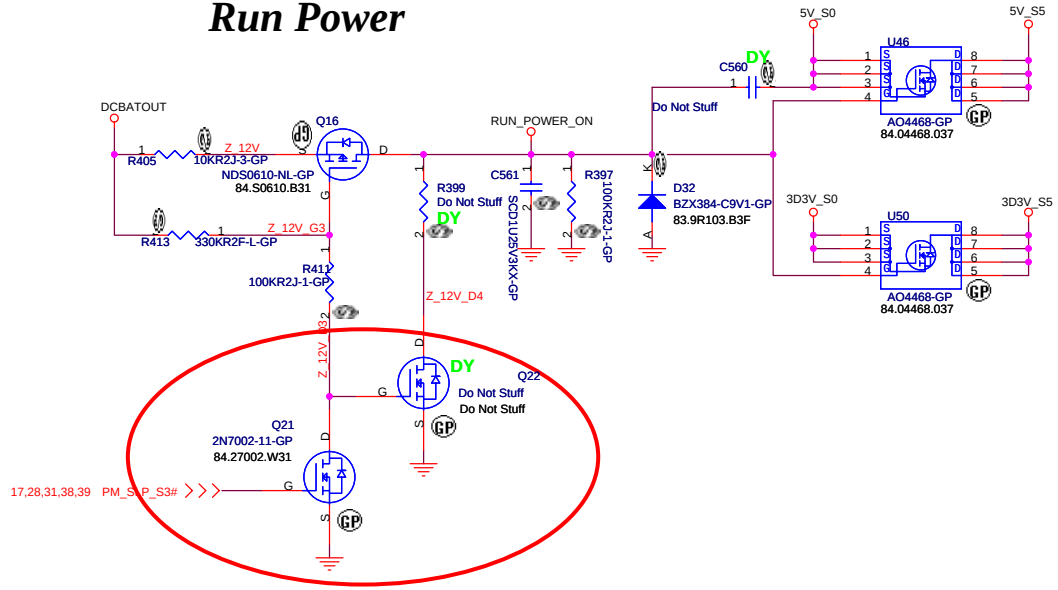
Date: Thursday, March 01, 2007 Sheet 33 of 42

Aux Power 3D3V_AUX_S5

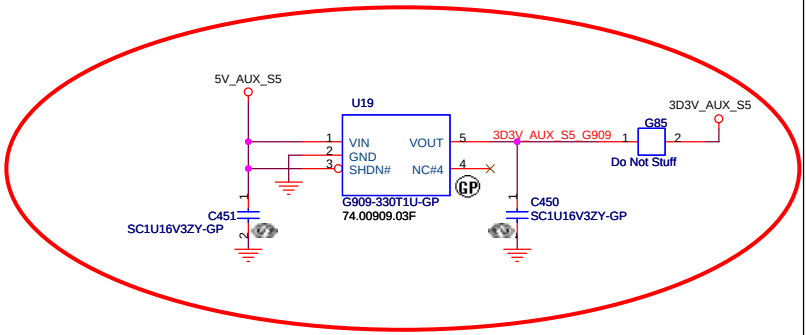




Run Power



Aux Power 3D3V_AUX_S5



SB modify

55.4H001.S03G

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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	Biwa	-1

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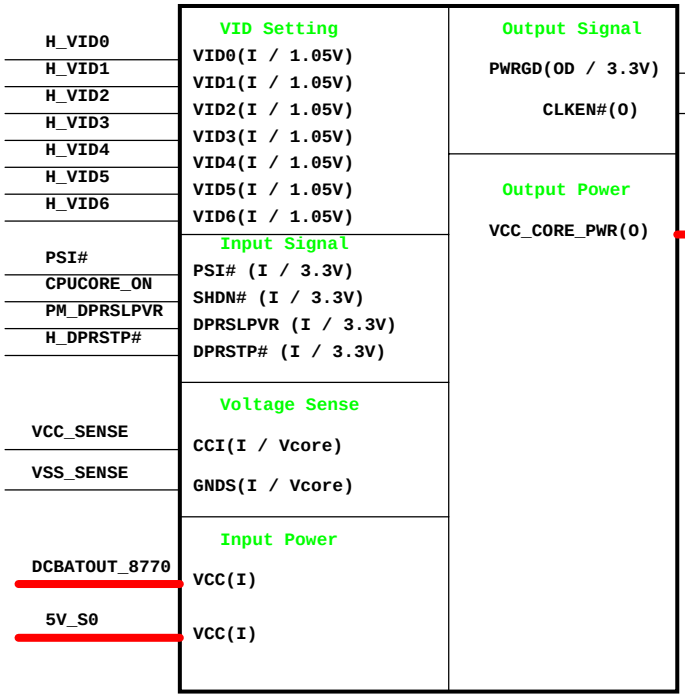
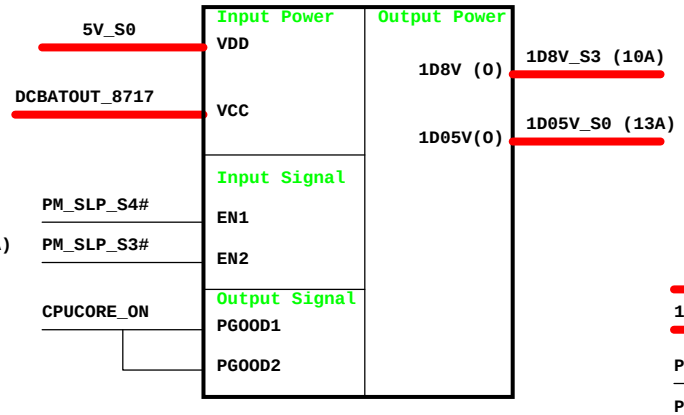
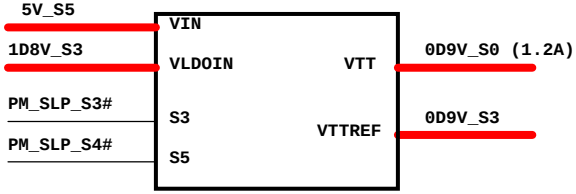
CPU_CORE
MAXIM MAX8770



MAX8717
1D8V/1D05V

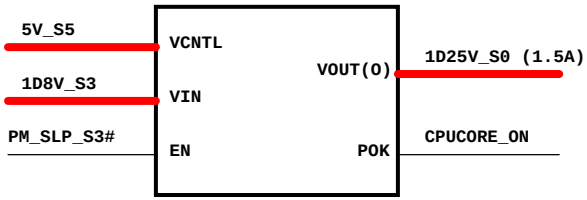


0D9V_S0



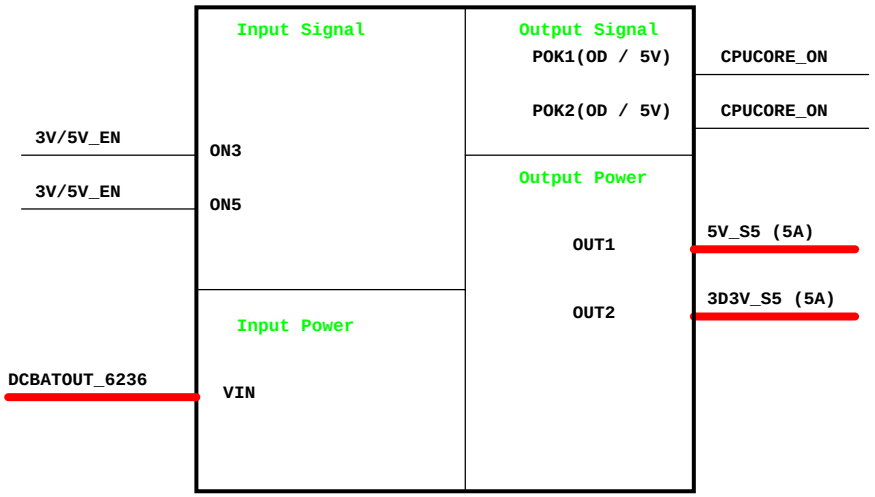
TPS51100

1D25V_S0

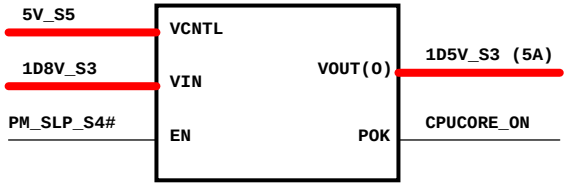


APL5915

ISL6236
5V/3D3V

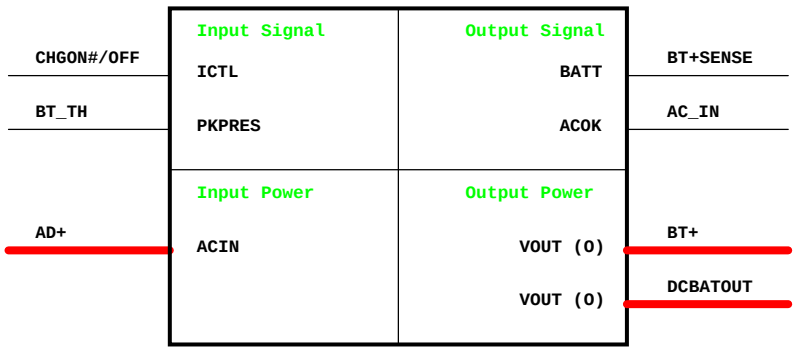


1D5V_S3



APL5912

Charger ISL6255



55.4H001.S03G

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	Biwa	SA

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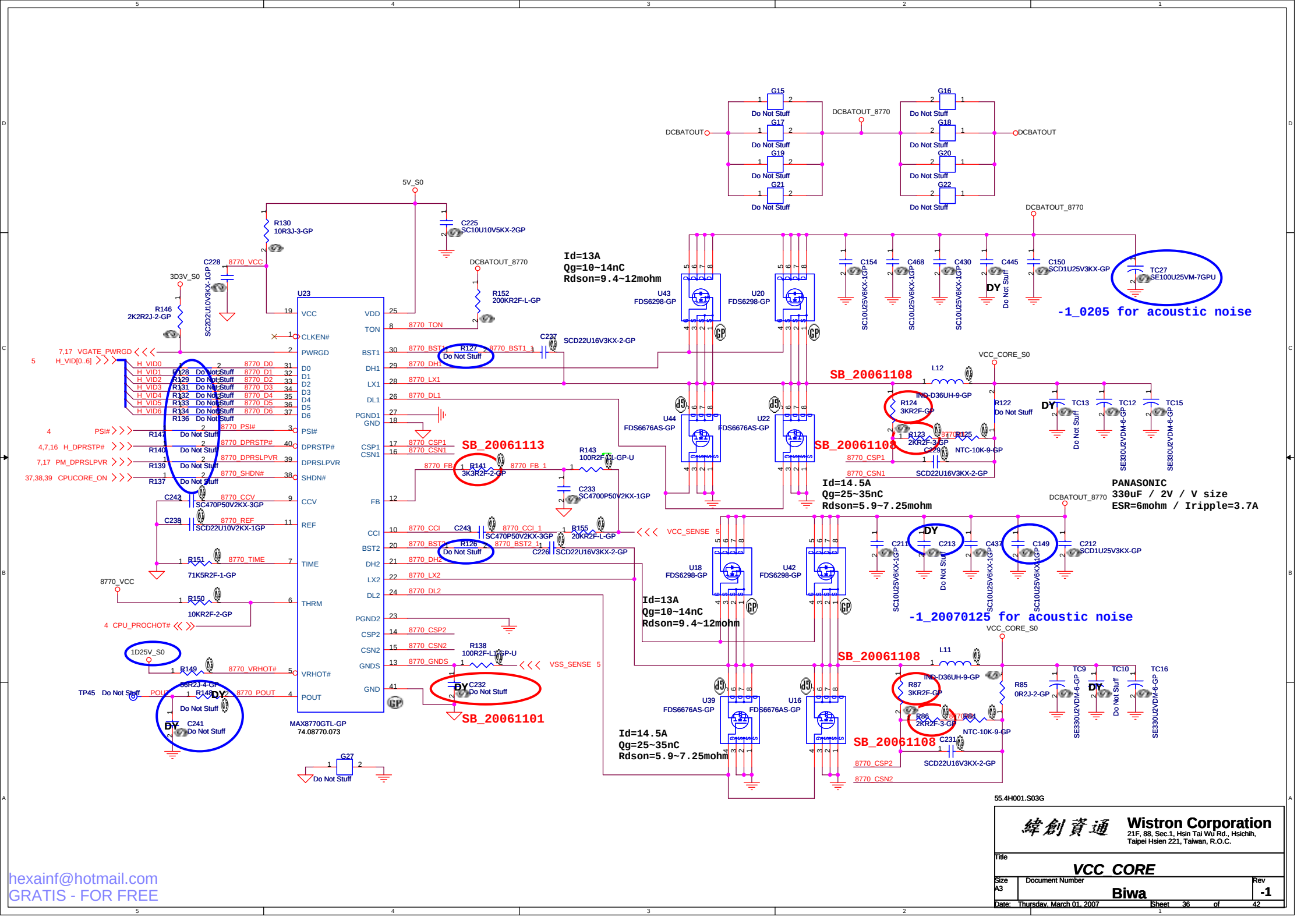
DCBATOUT
DCBATOUT_8770
Do Not Stuff
5V_S0
3D3V_S0
1D25V_S0
8770_VCC
U23
MAX8770GTL-GP
74.08770.073
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
SB_20061108
SB_20061113
SB_20061101
-1_0205 for acoustic noise
-1_20070125 for acoustic noise
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
VCC_CORE_S0
VCC_SENSE
VSS_SENSE
55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE
Biwa
Thursday, March 01, 2007
hexainf@hotmail.com
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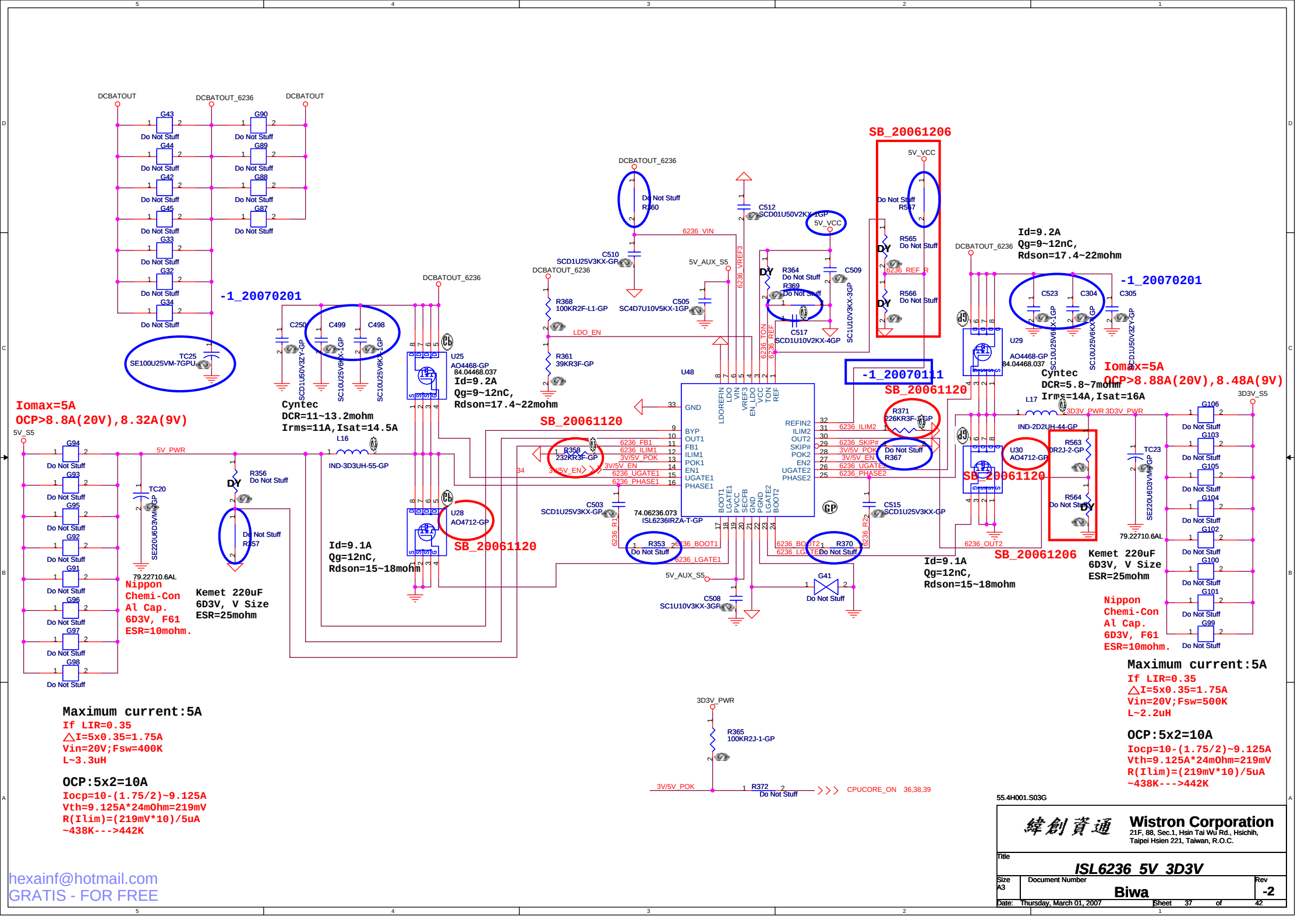

55.4H001.S03G

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Title: ISL6236 5V 3D3V

Size: A3 | Document Number: Biwa | Rev: -2

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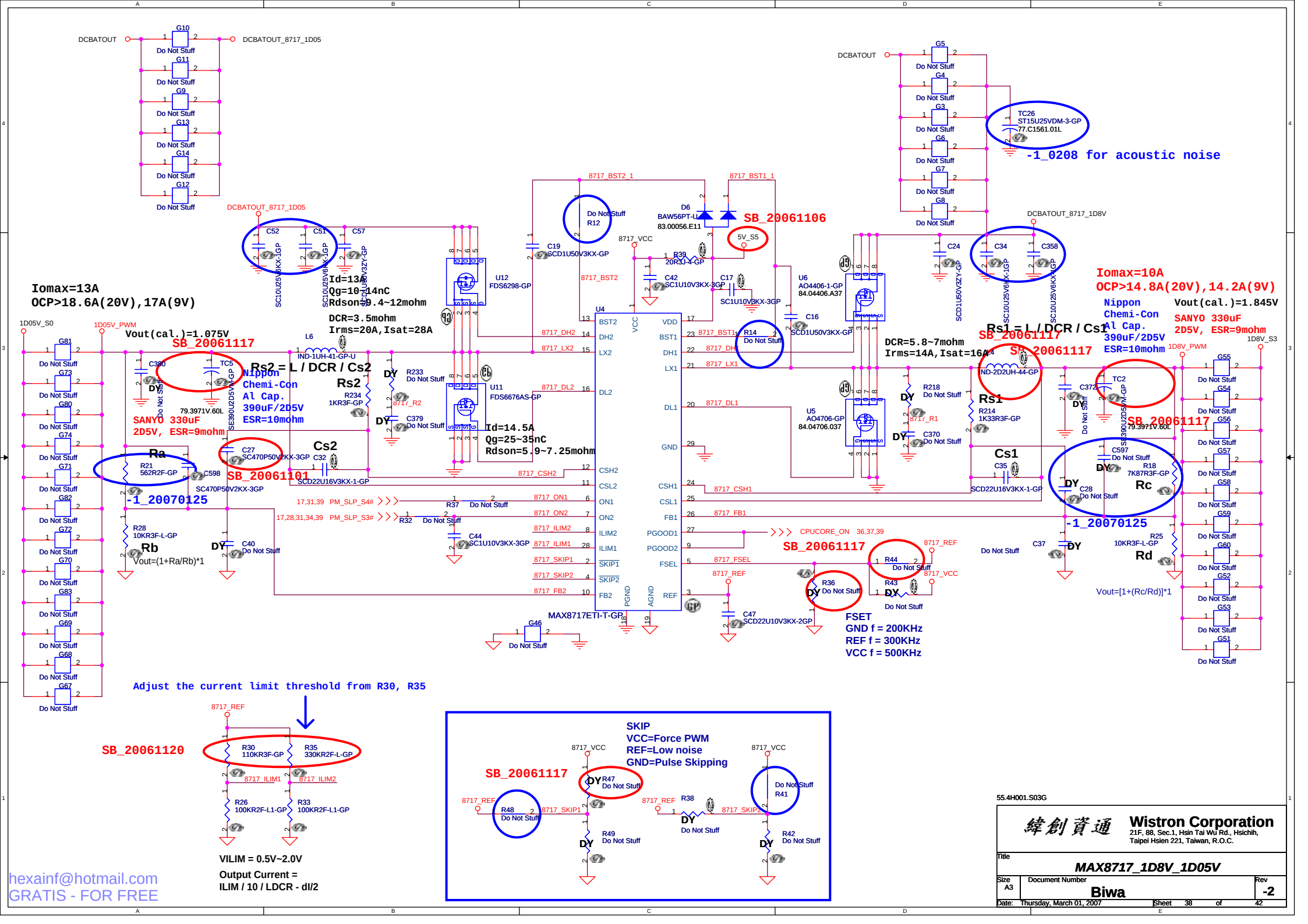
Iomax=13A
OCP>18.6A(20V),17A(9V)
Vout(cal.)=1.075V
SB_20061117
Rs2 = L / DCR / Cs2
Nippon Chemi-Con Al Cap. 390uF/2D5V ESR=10mohm
SANYO 330uF 2D5V, ESR=9mohm
Rs2
Ra
Rb
Vout=(1+Ra/Rb)*1
SB_20061101
-1_20070125
Cs2
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
DCR=3.5mohm
Irms=20A,Isat=28A
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
SB_20061106
MAX8717ETI-T-GP
Iomax=10A
OCP>14.8A(20V),14.2A(9V)
Vout(cal.)=1.845V
SANYO 330uF 2D5V, ESR=9mohm
Rs1 = L / DCR / Cs1
DCR=5.8~7mohm
Irms=14A,Isat=16A
Rs1
Cs1
Rc
Rd
Vout=[1+(Rc/Rd)]*1
-1_0208 for acoustic noise
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
Adjust the current limit threshold from R30, R35
SB_20061120
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
SB_20061117
hexainf@hotmail.com
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55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
MAX8717_1D8V_1D05V
Biwa
-2
Thursday, March 01, 2007
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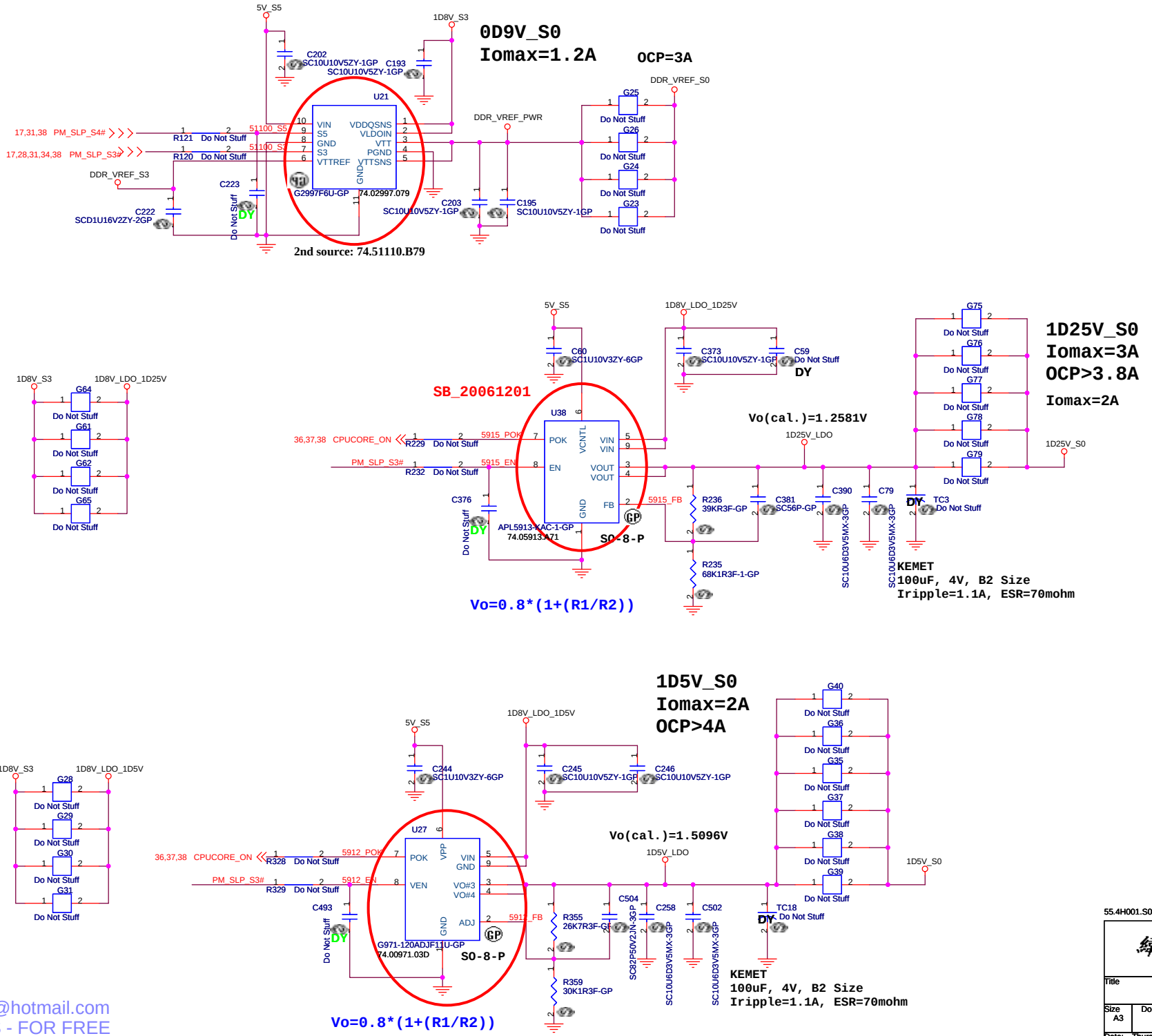
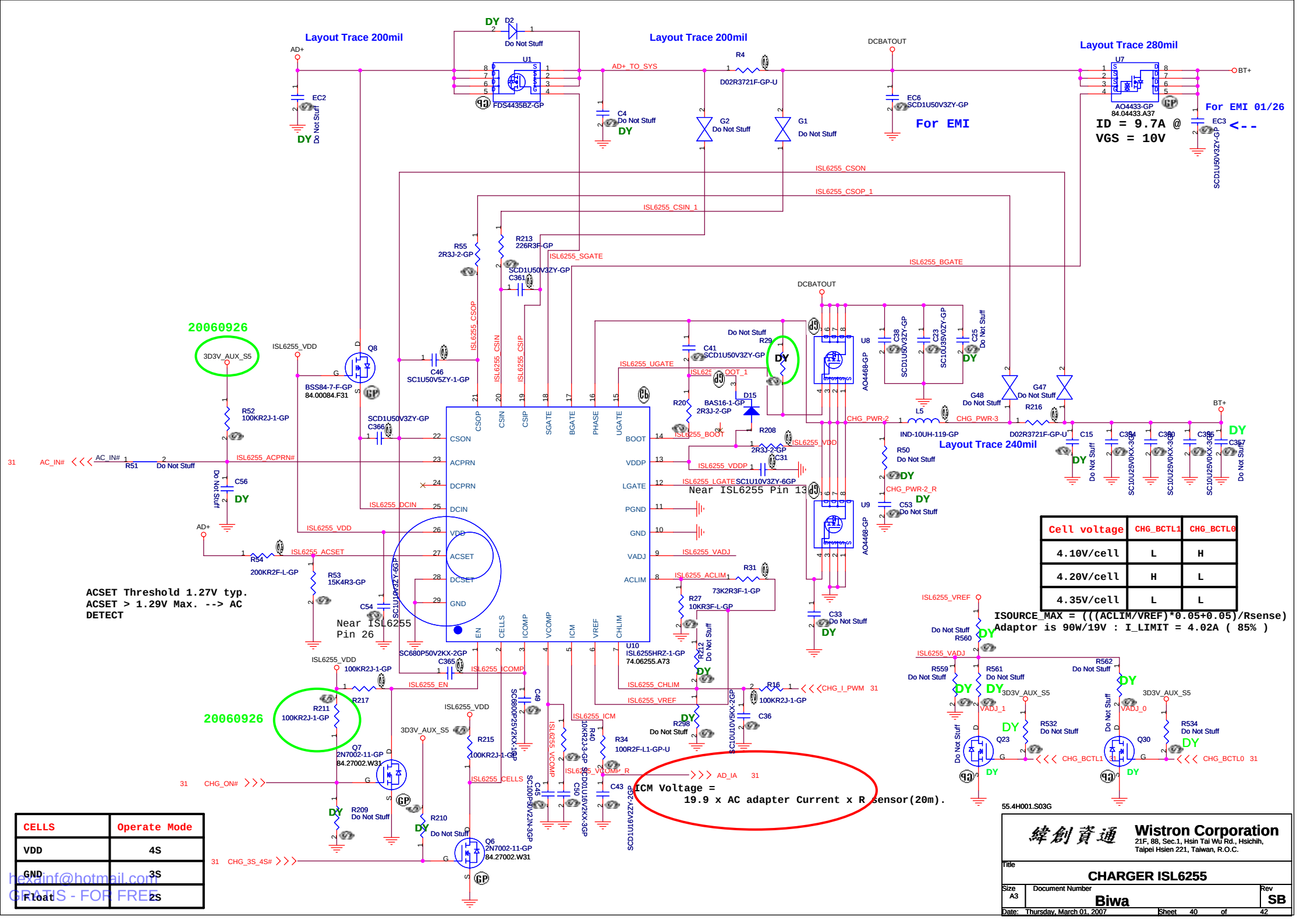
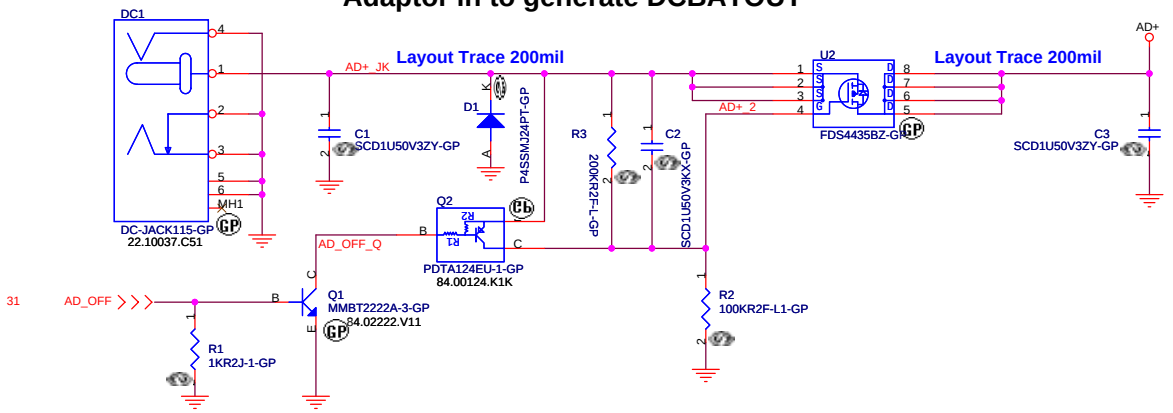
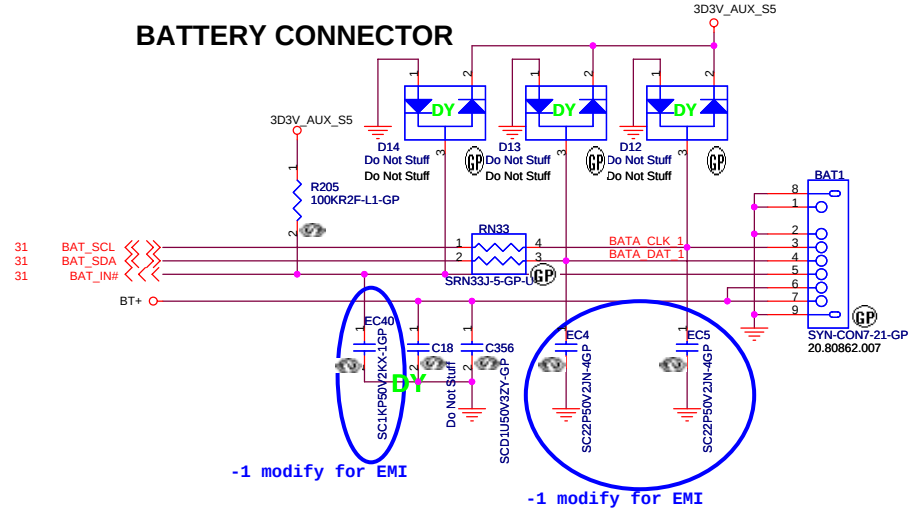




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



55.4H001.S03G

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	AD/BATT CONN	
Size A3	Document Number Biwa	Rev -1
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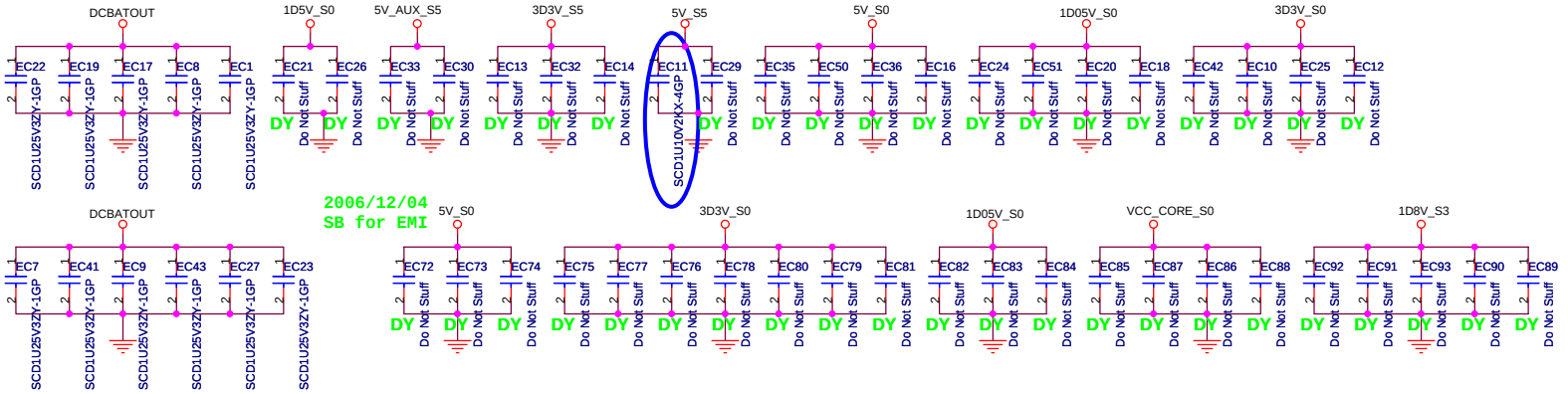
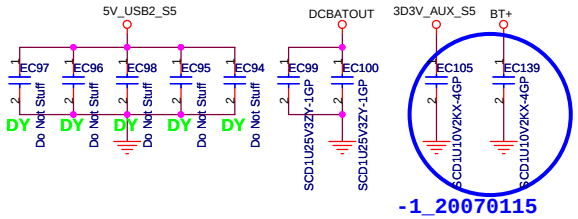
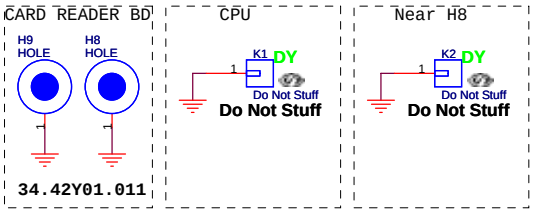
EMI Capacitor



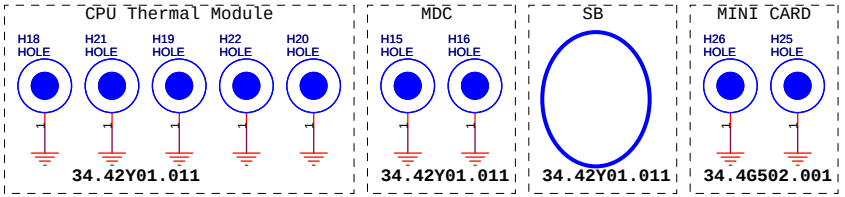


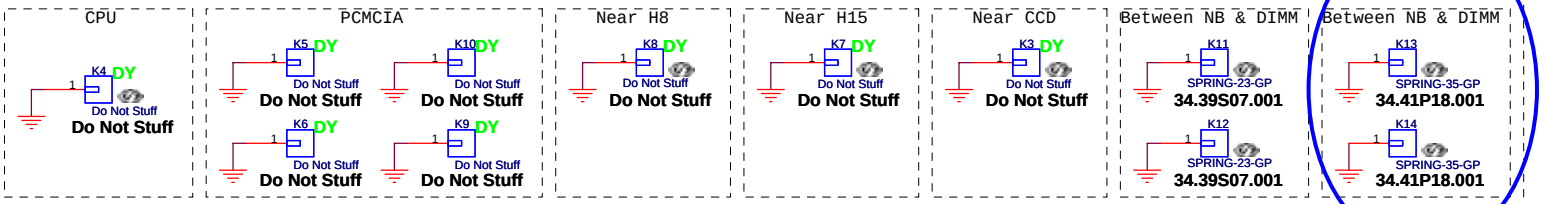
TOP

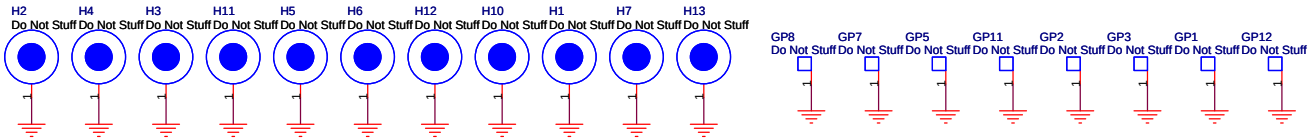


-1_0131 for thermal

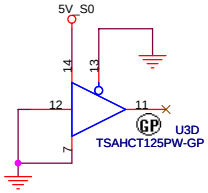
BOTTOM



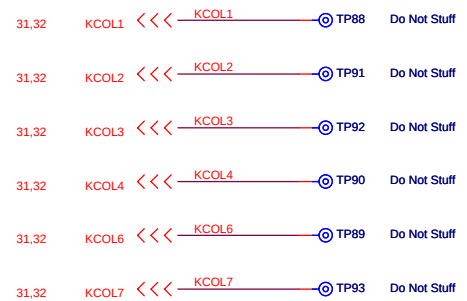




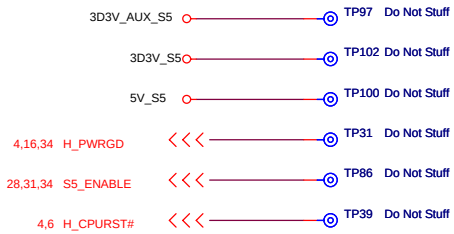
Unused gate



KBC JTAG Test Pad



DFX Test Point



Test Point放在Dimm Door打開可量測處

55.4H001.S03G

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